The characteristics of poly-silicon TFTs fabricated using ELA for AMOLED applications

Hyukjoo Son[1], Jaehong Kim[1], Sungwook Jung[1], Jeoungin Lee[1], Kyungsoo Jang[1], Hokyoon Chung[2], Byoungdeog Choi[2], Kiyong Lee[2], Junsin Yi[1]*

[1]School of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, Korea

TEL: +82-31-299-6570 , E-mail: dokbung@naver.com

[2]SAMSUNG SDI CO., LTD 428-5, Gongse-ri, Giheung-eup, Yongin-si, Gyeonggi-do 449-577, Korea

Keywords : poly-Si, ELA, glass, channel width

Abstract

In this paper, the properties of n-channel poly-Si TFTs with different channel widths are reported. Poly-Si fabricated using ELA on glass substrates has high quality as a material for applications such as TFT-LCDs. The fabricated n-channel TFTs have a double stack structure of oxide-nitride which acts as an insulator layer. The results show that the small channel TFTs exhibited a lower V_{TH} and the wide channel TFTs had a higher I_{DSAT}. The n-channel poly-Si TFTs with an I_{ON}/I_{OFF} value of more than 10^4 can be reliable switching devices for AMOLED displays.

1. Introduction

For applications such as system-on-panel devices, polycrystalline silicon (poly-Si) thin film transistors (TFTs) have recently been extensively studied for the fabrication of pixels, drivers, digital-to-analog converters (DACs), and timing controllers [1]. During the last few decades, the fabrication of poly-Si TFTs on glass substrates has been widely investigated for use in the active matrices of AMOLEDs [2]. It should be pointed out that, due to their relatively high field-effect mobility, poly-Si TFTs can be employed not only as switching-pixel transistors, but also for the integrated driving circuitry of AMOLEDs [3]. The transistors used as a current source in AMOLED pixel arrays have a bias at the drain terminal in addition to the gate, and have to occupy a very small area for the sake of achieving high brightness and resolution [4]. Poly-Si fabricated using excimer laser annealing (ELA) on glass has high-quality, which makes it a suitable material for applications such as TFT-LCD [5]. The use of a double-layer SiO_2/SiN_X film formed using plasma-enhanced chemical vapor deposition (PECVD) as a gate dielectric material for poly-Si TFTs was investigated, in order to reduce the mobile ion contamination and to improve the gate oxide integrity degradation [6]. In this study, the threshold voltage (V_{TH}), ON/OFF current ratio (I_{ON}/I_{OFF}) and saturation drain current (I_{DSAT}) of n-channel poly-Si TFTs with various channel widths were investigated, in order to assess the stability and enhancement of the TFT for as a driving circuit on glass. We investigated the quality of the n-channel poly-Si TFTs on glass substrate as a function of the channel width.

2. Experimental

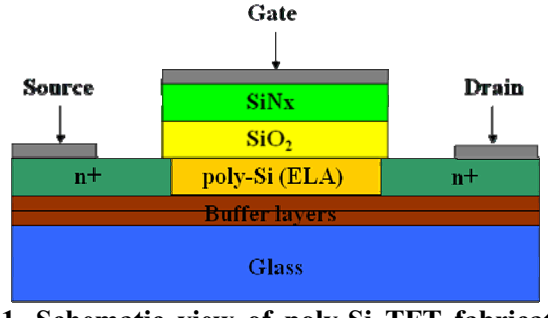

Fig. 1. Schematic view of poly-Si TFT fabricated using ELA on glass

A schematic view of the poly-Si TFT fabricated on glass using ELA is shown in Figure 1. We deposited a SiO_2 buffer layer on the glass substrates to fabricate

the low-temperature poly-Si (LTPS) TFTs. First, amorphous silicon films were deposited on the substrates by PECVD. Then, ELA was utilized to crystallize the amorphous silicon film. Subsequently, a gate-oxide layer (SiO_2) was formed by PECVD with tetraethylorthosilicate (TEOS)/O_2 gas. In addition to the silicon dioxide layer, an interposed SiNx film was deposited for some of the samples to prevent the incorporation of mobile ions into the SiO_2 gate insulator. The n^+ regions were created by ion doping. The LDD lengths were 1 μm. Contact holes were formed, and a source drain metal was deposited and patterned. Then, a passivation layer was deposited and patterned to complete the fabrication process. A schematic of the poly-Si TFT fabricated using ELA on glass substrate, incorporating the SiO_2/SiNx gate insulators, is shown in Figure 1. The devices used here had a channel length of 4 μm and various channel widths.

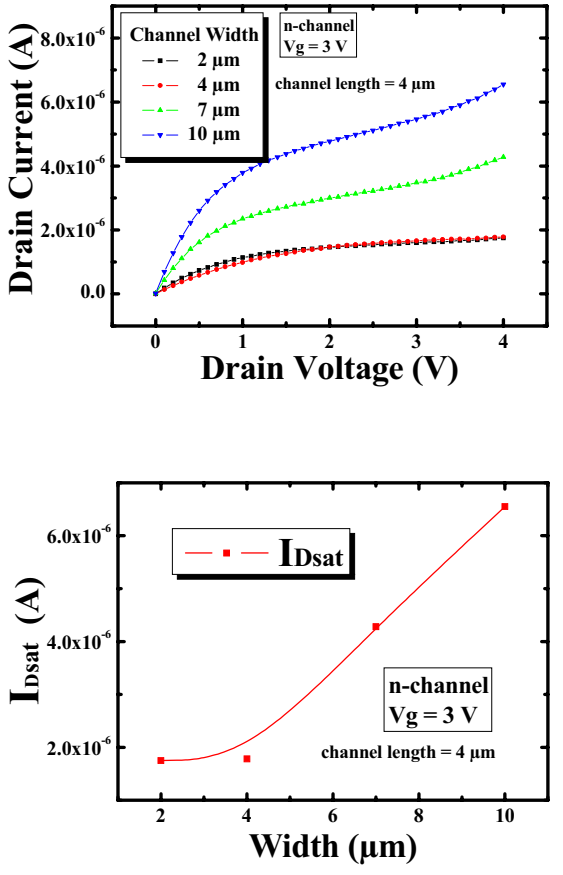

Fig. 2. Change of saturation drain current (I_{DSAT}), according to channel width

3. Results and discussion

As shown in Figure 2, we investigated the variation of I_{DSAT} with the channel width. The n-channel poly-Si TFTs with a relatively large channel width exhibited a higher I_{DSAT} than the ones with a small channel width when the drain bias was applied. However, the kink effect was decreased in the n-channel poly-Si TFTs with a small channel width. The fabricated n-type poly-Si TFTs with a small channel width have a low leakage current, which is an essential condition for high quality TFTs.

As shown in Figure 3, we investigated of V_{TH} and I_{ON}/I_{OFF} with the channel width. Figure 3 indicates that the poly-Si TFTs with a relatively small channel width exhibited a lower V_{TH} than the ones with a large channel width when the drain bias was applied. The characteristics show a high on-current, a good pinch-off and hard saturation, which are desirable for the practical application of the transistors. It is clearly visible that an increase in the channel width leads to a higher on-current and V_{TH}. It is clearly observed that the on-current (related to the intrinsic properties of the semiconductor) varies with an increase of the channel width.

The results show that the wide-channel poly-Si TFTs with an I_{ON}/I_{OFF} of more than 10^4 can be reliable switching devices for AMOLED displays.

4. Summary

The channel length of the fabricated poly-Si TFTs was kept constant, while their channel width was varied from 2 μm to 10 μm. The electrical parameters (V_{TH}, I_{ON}/I_{OFF}, I_{DSAT}) of the TFTs were studied. Although more studies are needed to clarify the variation of the properties of the TFTs with their channel length and width, it is clear that these parameters play an important role in determining their electrical properties. We believe that this research can provide the basic data required for applications based on TFTs for AMOLED displays.

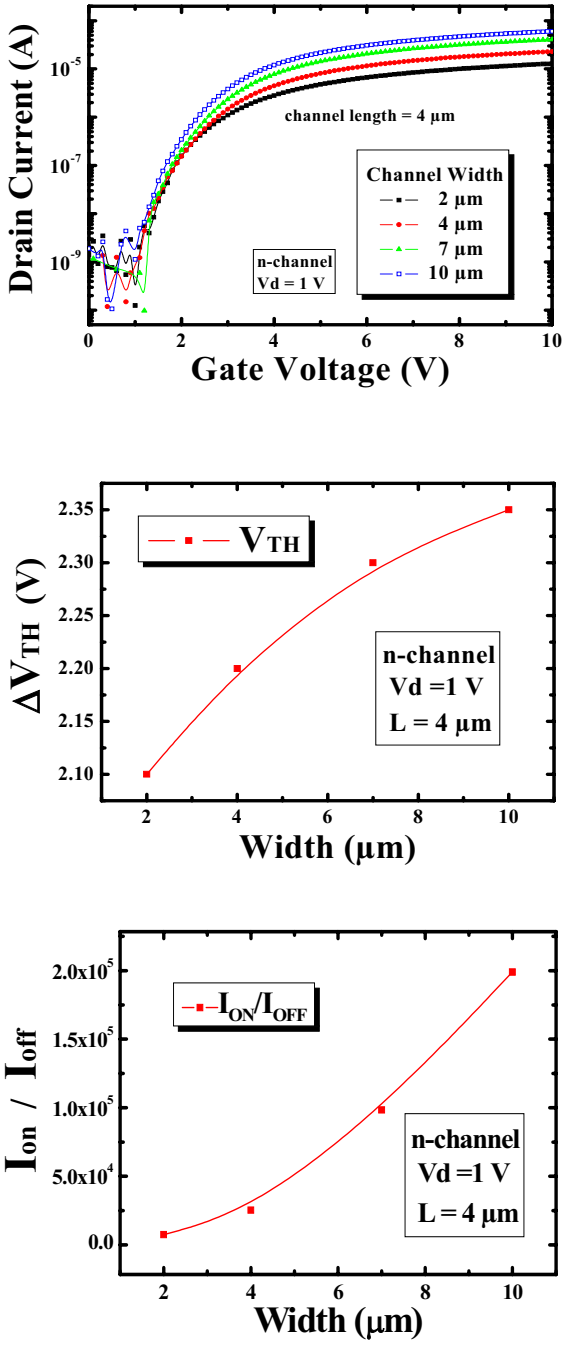

Fig. 3. Change of ON/OFF current ratio (I_{ON}/I_{OFF}) and threshold voltage (ΔV_{TH}), according to channel width

5. References

1. M. Stewart, R. S. Howell, L. Pires and M. K. Hatalis: IEEE Trans. Electron Devices 48 (2001) 845.
2. Y. Nishihara, S. Yamamoto, S. Yamada. T. Hikichi. I.Asai and T. Hamano, SID 92 DIGEST, p. 609 (1992).
3. W.-W. WU. A. G. Lewis, T.-Y. Huang and A. Chiang, SID 90 DIGEST, p. 311 (1990).
4. Kwang-Sub Shin, Jae-Hoon Lee, Sang-Myeon Han, In-Hyuk Song, Min-Koo Han. Non-Crystalline Solids 352 (2006) 1708–1710.
5. Myung-Sik Son, Keon-Ho Yoo, Jin Jang. Solid-State Electronics, 48 (2004) 2307–2313.
6. Byoung-Deog Choi, Won-Sik Kim, Myeong-Seob So, Jae-Bon Koo, Ramesh Kakkad, Yeon-Gon Mo, Sung-Chul Kim. Japanese Journal of Applied Physics, Vol. 44, No. 9A, 2005, pp. 6417–6420.