Concept of Effective Gate-Source Overlap Length in Inverted-staggered TFT Structures

Keum-Dong Jung, Yoo Chul Kim, Byeong-Ju Kim, Byung-Gook Park, Hyungcheol Shin, and Jong Duk Lee

Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National University, Seoul 151-742, Korea

TEL:82-2-880-7282, e-mail: windbit@naver.com

Keywords : effective overlap length, inverted-staggered, top-contact, TFT

Abstract

Analytic equations are derived from physical quantities in the gate-source overlap region and the concept of effective gate-source overlap length is proposed. The effective overlap length can be affected by gate voltage, insulator thickness and semiconductor thickness, and the overlap length should be larger than the length to obtain maximum driving current.

1. Introduction

Gate-source or gate-drain overlap region in inverted-staggered(top-contact) thin-film transistors has been known to be related to the source/drain series resistances of the device[1,2]. If the overlap length becomes shorter, total driving current reduces because the series resistance becomes larger. The effects of overlap length become even more important as the channel length scales down to obtain high driving current. However, there has been no effort to understand the current flow in the overlap region, so no appropriate model or equations have been proposed. In this paper, using physical quantities and simple assumptions, an equation for the current flow in the overlap region is derived, and the meaning of the equations is discussed using the concept of effective gate-source overlap length.

2. Analysis

A hydrogenated amorphous silicon TFT is assumed for the analysis of inverted-staggered TFTs as shown in Fig. 1. For the linear regime operation, the gate electrode is biased to positive voltage to accumulate charges in the channel and the drain electrode is biased to 0.1 V. Under the bias condition, the sheet resistance R_{sh} of the accumulation layer which is formed not only in the channel but also at the bottom

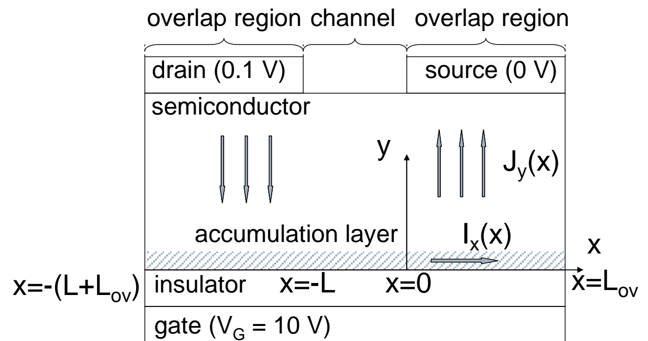

Fig. 1. Device structure to be analyzed.

of overlap region can be considered uniform because it is mainly determined by the gate voltage V_G. For further analysis, two assumptions are made: One assumption is that the current in the overlap region flows from the channel to the source electrode only in y-direction as represented by current density $J_y(x)$. The other assumption is the x-direction conduction only occurs in the accumulation layer, which is represented by $I_x(x)$. R_y represent the resistance per unit area in y-direction, which includes both of bulk resistance of semiconductor and contact resistance. V(x) represents the potential in the accumulation layer.

Using the above assumptions and physical quantities, one can obtain the following three equations.

$$I_x(x) = W\int_x^{L_{ov}} J_y(x)dx \qquad (1)$$

$$V(x) - (J_y(x)Wdx)\frac{R_y}{Wdx} = 0 \qquad (2)$$

$$V(x+dx) = V(x) - I_x(x)R_{sh}\frac{dx}{W} \qquad (3)$$

If R_y and R_{sh} is known, the equations can be solved easily for $J_y(x)$ as

$$J_y(x) = J_{y0}\left[\cosh(-\frac{x}{L_0}) + \tanh(\frac{L_{ov}}{L_0})\sinh(-\frac{x}{L_0})\right] \qquad (4)$$

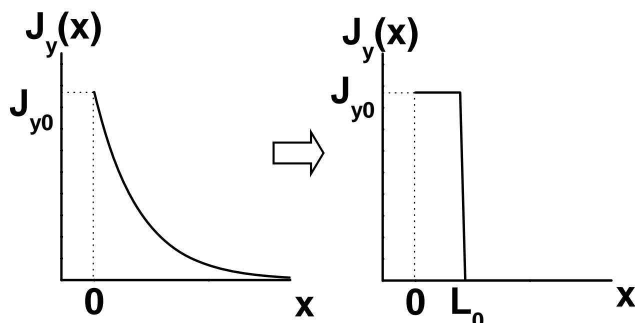

Fig. 2. The current density in the overlap region decays exponentially with maximum value of J_{y0} at x=0 and characteristic length of L_0.

$$L_0 = \sqrt{R_y / R_{sh}} \qquad (5)$$

where L_0 represents the effective gate-source overlap length and J_{y0} represents the maximum y-direction current density. If L_{ov} is assumed to be much larger than L_0, $J_y(x)$ becomes

$$J_y(x) = J_{y0} \exp(-x/L_0) \;\; when \;\; L_{ov} >> L_0 . \qquad (6)$$

According to the derived equation, the y-direction current density is maximum at x=0 and decays exponentially with the characteristic length L_0. Total current I_{tot} also can be represented using L_0 and J_{y0}, that is, $I_{tot} = W\int_0^{\infty} J_y(x)dx = WL_0 J_{y0}$, so it can be considered that constant current flows in overlap region with current density J_{y0} and overlap length L_0 as shown in Fig. 2.

Because L_0 is a function of R_{sh} and R_y, it can be changed with material, fabrication method or bias condition. R_{sh} can be changed by gate voltage, threshold voltage, insulator capacitance and mobility whereas R_y is affected by bulk semiconductor properties and contact quality. If gate voltage, insulator capacitance and mobility become larger to obtain small R_{sh}, L_0 is expected to become larger. If film thickness becomes thicker and contact quality becomes worse, L_0 also becomes larger due to larger R_y.

3. Verification & Discussion

$J_y(x)$ and L_0 can not be measured easily with experiment, so device simulation with SILVACO™ simulator is used for the verification of derived equations. Back channel etched amorphous silicon TFT structure is used for the simulation. The thicknesses of silicon nitride, amorphous silicon and n^+ layer are 400 nm, 150 nm and 30 nm, respectively.

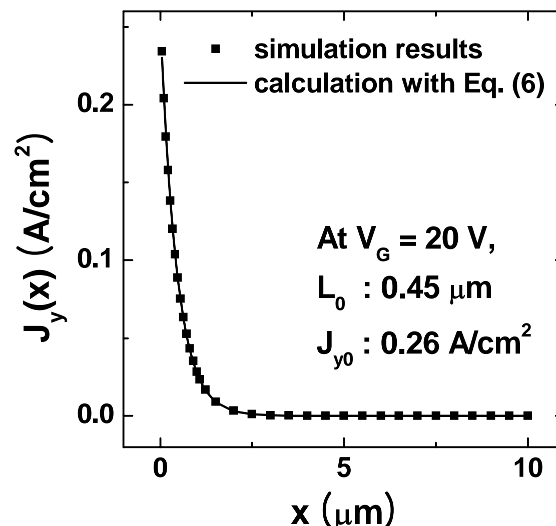

Fig. 3. From the simulation, $J_y(x)$ is obtained. L_0 and J_{y0} can be extracted from $J_y(x)$ using Eq. (6).

The thickness of the amorphous silicon channel is 50 nm. The channel length L and the overlap length L_{ov} is 2 μm and 10 μm, respectively. The effective overlap length L_0 is extracted from $J_y(x)$ which is obtained from the simulation. As shown in Fig. 3, reasonable L_0 and J_{y0} can be extracted from $J_y(x)$ and Eq. (6).

In Fig. 4, the relation between L_0 and other parameters are shown. As expected in previous discussion, L_0 increases with the increase of the gate voltage V_G and the insulator capacitor C_i because R_{sh} decreases in those conditions. If the semiconductor

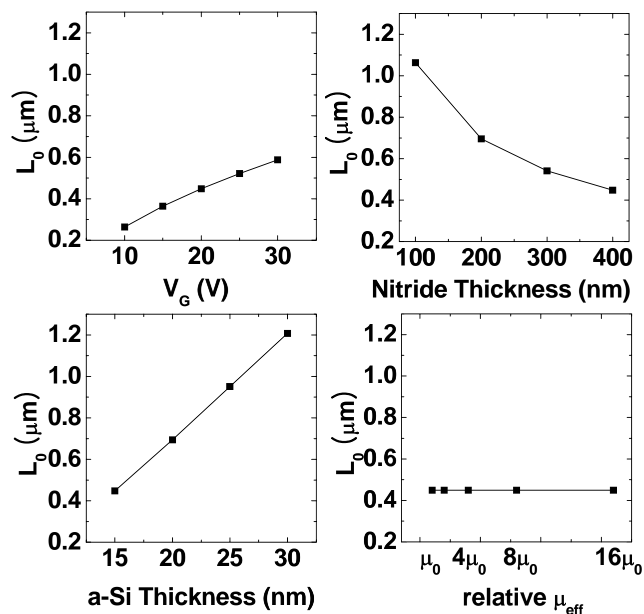

Fig. 4. The relations between L_0 and other device parameters.

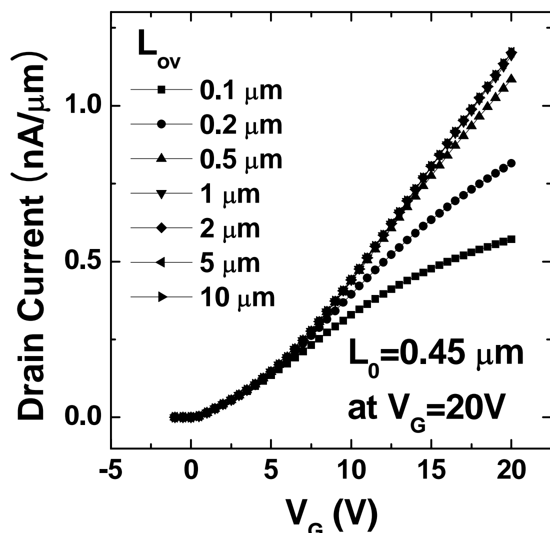

Fig. 5. If the overlap length L_{ov} becomes similar or smaller than L_0, the drain current start to decrease.

thickness is increased to increase R_y, L_0 also increases as predicted by Eq. (5). However, L_0 does not increase with the change of field effect mobility because R_{sh} and R_y decreases together in that case.

In the above discussion, L_{ov} is assumed to be much larger than L_0, so that the effect of the hyperbolic tangent term in Eq. (4) becomes negligible. However, if L_{ov} becomes smaller than L_0, $J_y(x)$ in Eq. (4) can decrease, so that the on-current of the device can be restricted by the insufficient overlap length. The I-V characteristics for the devices with different L_{ov} are shown in Fig. 5. For V_G smaller than 7 V, the drain current is almost the same because L_0 is always smaller than the minimum L_{ov} (0.1 μm). For V_G of 20 V, the drain currents are almost the same if the L_{ov} is larger than 1 μm. However, for L_{ov} of 0.5 μm which is similar to L_0 at V_G of 20 V, slight on-current degradation is observed. For even more narrow L_{ov}, the drain current reduces severely. Therefore, it is better to maintain L_{ov} to be larger enough than L_0 to obtain maximum on-current. In addition, because L_0 can be changed by several conditions, the maximum L_0 value should be obtained and used for device design.

4. Summary

The concept of effective gate-source overlap length is derived from analytical equations and its implications are discussed. The effective length depends on various parameters, e.g., gate voltage, insulator capacitance and semiconductor thickness. If the device overlap length L_{ov} is smaller than the effective overlap length L_0, the on-current can be reduced by the insufficient overlap length. Therefore, device designers should consider the maximum effective overlap length to obtain maximum driving current. These results can be used to all the inverted-staggered structure TFTs including a-Si TFTs, poly-Si TFTs, ZnO TFTs, and top-contact OTFTs.

5. References

1. Shengwen Luan et al, Journal of Applied Physics, 72, pp. 766-772(1992).
2. C.-Y. Chen et al, Solid-State Electronics, 42, pp. 705-713(1998).