Performance of Thin Film Transistors Having an As-Deposited Polycrystalline Silicon Channel Layer

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Abstract

Polycrystalline silicon (poly-Si) films were prepared directly on plastic substrates at a low (< 200°C) by using Catalytic Chemical Vapor Deposition (Cat-CVD) technique without subsequent annealing steps. Surface roughness of the poly-Si layer and the density of the gate dielectric layer were found to be influential to the TFT performance.

1. Introduction

Catalytic chemical vapor deposition (Cat-CVD) has attracted a great deal of attention as a fabrication technique for thin films of semiconductors and insulators, having advantages of the high deposition rate and the capability of growing electronic-quality films[1,2). Because of meta-stability in a-Si:H, which deteriorates its electrical properties upon light exposure or bias application, as well as its low carrier mobility, polycrystalline silicon (poly-Si) is currently being investigated as a next candidate for many of these device applications[3)]. Currently, the crystalline silicon films are fabricated in the two-stage process of amorphous film deposition followed by laser annealing[4)]. A lot of research efforts have been devoted to form crystalline phase in a single step with a high deposition rate and a low process temperature[5,6)].

The as-deposited poly-Si films usually have a high degree of surface roughness which in turn affects the nucleation and growth of the overlaying layers. Therefore, performance of the top-gate type thin film transistor (TFT) having the as-deposited poly-Si film as a channel layer is greatly influenced by the morphology and density of the gate dielectric layer. In this study, the poly-Si channel layer was deposited directly by the Cat-CVD technique without the subsequent crystallization step, and the silicon dioxide gate dielectric layer was fabricated by ICP-CVD. All the process temperatures were maintained below 200℃.

2. Experimental

The as deposited poly silicon films were prepared by using a Cat-CVD system. The tungsten wires (filament) with 0.4mm diameter and 50mm length were used as a catalyst and placed over the substrate at a distance of 50mm. The filament temperature was measured by a pyrometer. The temperature of the substrate was monitored by a thermocouple (TC) attached on the substrate holder.

The main deposition parameters are listed in Table I. The as-deposited poly silicon films have been deposited at a low substrate temperature (<200℃).

Table I. Cat-CVD Deposition Parameters

Variable Parameters	Catalyst temperature (°C)	1740, 2000, 2200
	Hydrogen dilution ratio (%)	60, 75, 90
	Gas pressure (mTorr)	20, 40, 60
	Film thickness (nm)	50, 100, 150, 200
Fixed Parameters	Substrate temperature (°C)	190

The film thickness was determined by a surface profilometer (alpha-step). The structure of the films was studied X-ray diffraction (XRD) using copper (Cu) Kα X-rays. The hydrogen content of the films was estimated by Fourier–Transformed Infrared spectroscopy (FTIR). The crystallinity and roughness of the films were investigated by Raman scattering spectroscopy and UV reflectance spectroscopy. Raman spectrum around the crystalline silicon transverse optical (TO) peak was deconvoluted into their integrated crystalline Gaussian peak, I_c(~520cm^{-1}), amorphous Gaussian peak, I_a(~480cm^{-1}), and intermediate Gaussian peak, I_m(~510cm^{-1}). The crystalline volume fraction (X_c) of the as deposited poly silicon films was estimated as follows:

$$X_c = (I_c+I_m)/(I_c+I_m+I_a)$$

N-type top-gate TFTs have been processed by using as-deposited poly silicon film as an active layer. The film was deposited by Cat-CVD. The channel width and length were 20 μm, respectively. A buffer layer and gate insulator were deposited using ICP-CVD of high density plasma at 170˚C, and gate metal was deposited using an E-beam evaporator. Activation annealing was performed using a self-aligned excimer laser annealing (ELA) after the gate dopant using ion implantation. All process temperatures were kept below 200˚C so as to apply to the plastic substrate in the future.

3. Results and Discussion

As-deposited poly silicon films having a high deposition rate (~35Å/sec) and a high crystallinity were prepared successfully at process parameters of a high filament temperature, a high hydrogen dilution ratio and a low chamber pressure. Enhancement of the crystalline volume fraction was observed as the chamber pressure decreased and the hydrogen dilution ratio increased. Fig. 1 shows the Raman spectra of the as-deposited poly silicon films prepared at various conditions. As shown in Fig. 1(a), the film is in the amorphous phase when the filament temperature is low, and the crystalline peak grows as the filament temperature rises. Fig. 1(b) shows that the crystalline phase increases with the chamber pressure. In Fig. 1(c), it looks as if the crystallinity increases with the hydrogen dilution. However, the crystalline volume fraction that was estimated from the relative intensity values of the amorphous, intermediate phase, and crystalline peaks increases with the hydrogen.

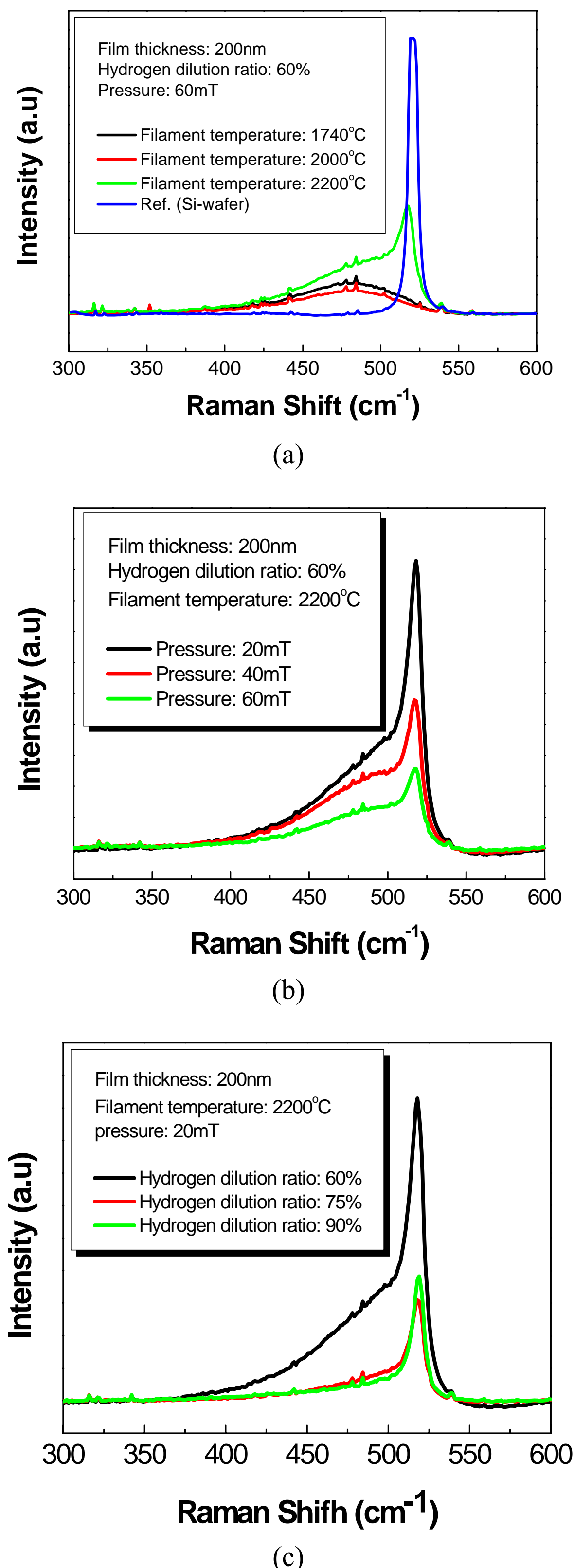

Fig. 2 Raman spectra of the as-deposited poly silicon films prepared at different process conditions: (a) filament temperature (b) process pressure (c) hydrogen dilution ratio

Fig. 2 shows X-ray diffraction spectra of the as-deposited poly silicon films. The X-ray analysis showed a dominant peak at a Bragg angle that corresponding to the (111) plane. This result indicates that the crystallites have a columnar structure growing preferentially along the <111> direction. The preferred growth orientation did not change with the filament temperature, while the degree of crystallinity is influenced greatly by the filament temperature as shown in Fig. 1(a). The as-deposited poly silicon films showed polycrystalline phase even as the thickness was reduced to 50 nm.

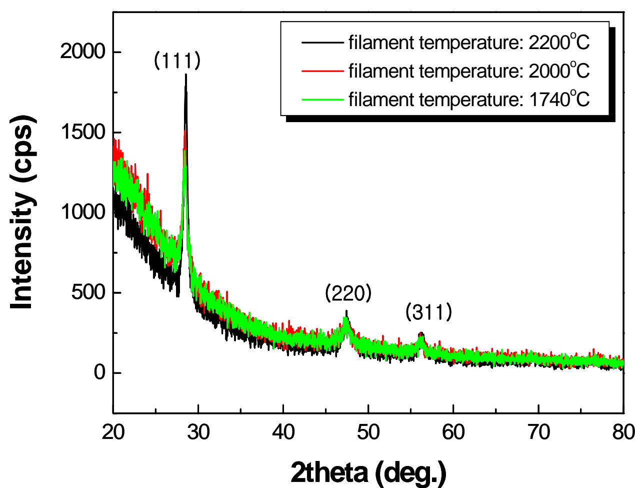

Fig.2 X-ray Diffraction Spectra of the poly silicon films prepared at various temperatures. Hydrogen dilution ratio was 90%

N-type top-gate TFTs were fabricated with the Cat-CVD as-deposited poly-Si and ICP-CVD SiO_2 layers. The TFT transfer characteristic curve is shown in Fig. 3. The drain current – gate voltage relationship of the resulting TFT shows a noticeable shift of the threshold voltage (V_{th}), and an increased value of the off-current, as the gate voltage sweep went on. When the TFT is fully stabilized, we obtained a mobility of ~30cm^2/Vsec, a threshold voltage of 4.5 V, and a subthreshold slope of 0.54V/decade.

Fig. 4 shows a cross-sectional TEM image of the TFT. The incubation layer thickness was much smaller than that of the poly silicon layer, so the instability in the TFT transfer characteristic can be ruled out. However, it is seen in the figure that the SiO_2 gate dielectric layer has a columnar morphology following the topography of the poly silicon layer. We can deduce that a high density of charge traps exist along the boundary of columns inside the gate dielectric layer. These traps seem to be stabilized through repeated cycles of gate voltage sweeps before the gate bias can be effectively transferred to the channel region. Annealing at an elevated temperature cannot be an option for reducing the trap density since we aim at the development of TFTs on plastic substrates.

In order to investigate this instability phenomenon further, we compared the transfer characteristic of the as-deposited poly silicon TFT with that of a laser-crystallized poly silicon TFT.[7]

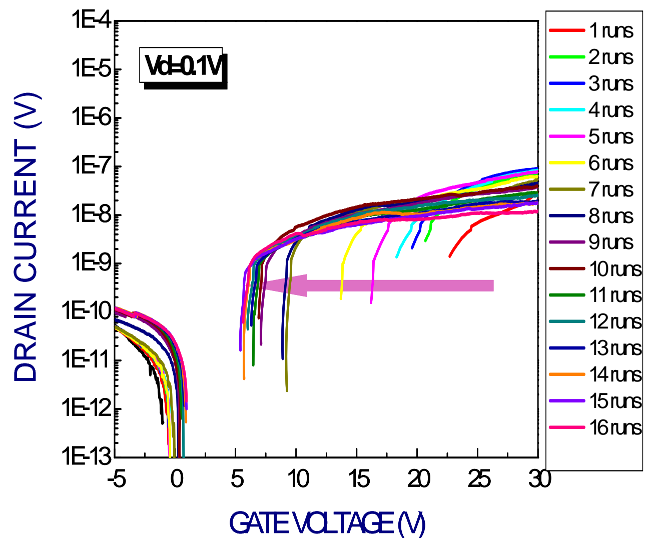

Fig. 3 Transfer characteristic curve of the TFT having an as-deposited poly silicon film as a channel layer

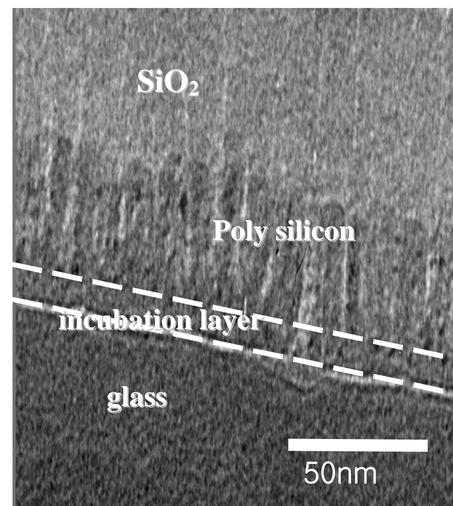

Fig. 4 Cross sectional TEM image of the SiO_2 gate dielectric and poly silicon channel region in a top-gate coplanar type TFT.

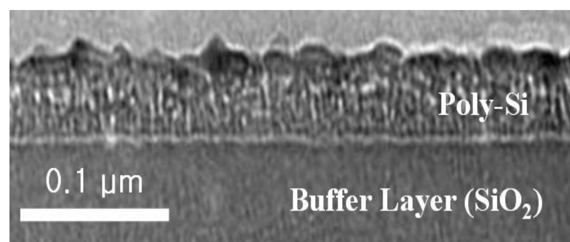

Fig. 5 Cross sectional TEM image showing the interface between the laser-crystallized poly silicon channel layer and the SiO_2 gate dielectric layer

Fig. 5 shows the cross sectional TEM image of the poly silicon TFT prepared by excimer laser annealing (ELA) of amorphous silicon films. We see that grains bigger than the columns of as-deposited poly silicon are formed at the interface with the gate dielectric layer, and there is no sign of columnar growth of the SiO_2 layer.

Fig. 6 shows the transfer characteristic curve of the TFT prepared with the ELA poly silicon layer. No hysteresis was observed during the gate voltage sweep. Also, the threshold voltage was decreased to 1.65 V, indicating that the leakage through the gate dielectric layer was much reduced. This result suggests that a homogenous growth of the gate dielectric layer is critical to the performance of the top-gate transistors. Therefore, it is very important to devise a practical method to produce a smooth surface of the poly silicon layer, other than laser annealing, in order to obtain a stable on-off behavior of the transistor.

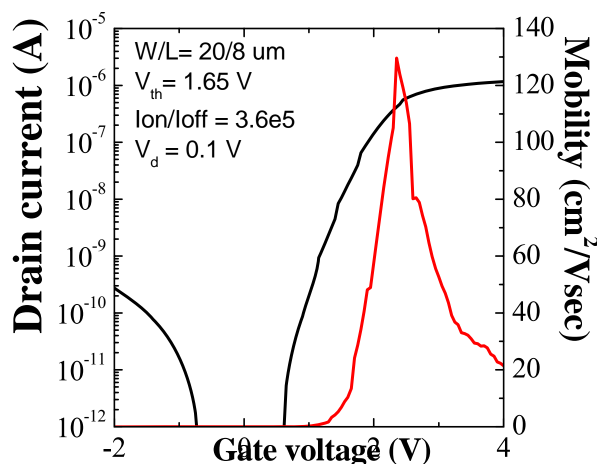

Fig. 6 Transfer characteristic curve of the TFTs prepared with laser-crystallized poly silicon channel layer and ICP-CVD gate dielectric layer.

4. Summary

This research showed that highly crystalline poly-Si films could be prepared successfully on plastic substrates at a low (< 200°C) by using Catalytic Chemical Vapor Deposition (Cat-CVD) technique without subsequent annealing steps. Effects of various process parameters on the as-deposited poly-Si films were investigated. N-type top-gate thin-film transistors were fabricated using the direct-deposited poly-Si films. We obtained a high mobility of ~30cm^2/Vs and a subthreshold slope of 0.54V/decade. We need to find a practical method to produce a smooth surface of the as-deposited poly silicon film so that the gate dielectric layer can grow homogeneously on it. If matched with a good dielectric layer, the low temperature poly-Si films prepared directly by Cat-CVD can be a promising material as an active layer of thin film transistors for driving active matrix organic light emitting displays (AM-OLEDs) on plastic substrates.

5. Acknowledgement

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6. References

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