Channel Orientation Dependent Electrical Characteristics of Low Temperature Poly-Si Thin-film Transistor Using Sequential Lateral Solidification Laser Crystallization

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Abstract

The electrical characteristics of low temperature poly-Si (LTPS) thin-film transistors (TFT) with channel parallel and perpendicular to the direction of lateral growth were studied. The poly-Si film was crystallized using sequential lateral solidification (SLS) laser crystallization technique. The channel orientation dependent turn-on characteristics were investigated by using gated-diodes and capacitance-voltage measurements

1. Introduction

Poly-Si using SLS crystallization technique has advantages over ELA such as larger grain size, higher carrier mobility and better device uniformity [1]-[3]. However, the electrical characteristics of SLS TFTs strongly depend on the direction of lateral growth with respect to channel direction [4]. This orientation dependent electrical characteristic will restrict the layout freedom of integrated peripheral circuits and pixel circuits for display application. In this work, the electrical characteristics of TFTs with channel parallel to and perpendicular to the direction of lateral growth as shown in Fig.1 were studied by using gated-diode measurement. Capacitance-voltage characteristic was also performed to study the orientation dependent electrical characteristic of SLS TFTs.

2. Experimental

Top gate n-type and p-type TFTs were fabricated on 370mm×470mm glass substrate by LTPS processes. Initially, 300nm-thick TEOS buffer SiO_2 and 50 nm-thick amorphous silicon (a-Si:H) films were deposited on bare glass by PECVD. The a-Si:H films were then dehydrogenated by furnace annealing at 400 °C. After dehydrogenation, the a-Si films were then crystallized by 2-shot SLS [1]-[2]. The poly-Si film was then patterned to form islands with TFT channel orientation perpendicular or parallel to the direction of SLS lateral growth. 100nm-thick gate oxide was then deposited by PECVD. MoW was sputtered to form the gate and source/drain metal line and plasma ion doping was used to form source/drain regions. No post hydrogenation annealing was performed in order to reflect the real influence of grain boundary traps on the device characteristics. The TFT dimension measured in this work was W = 8 μm with L = 4~16 μm. All the I-V characteristics were measured by computer-controlled Agilent 4156C semiconductor parameter analyzer and HP4284A LCR meter.

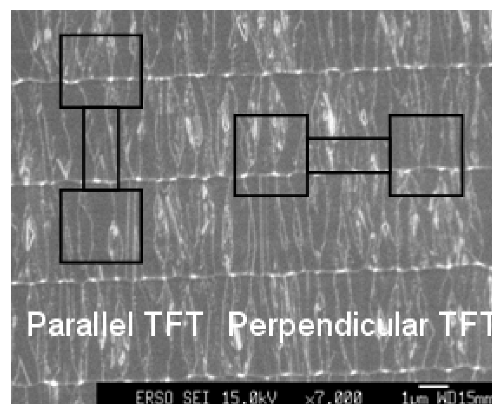

Fig. 1 Schematic view of SLS TFT devices with different channel orientation

3. Results and discussion

(1). Capacitance-voltage characteristics

Fig. 2 shows the C-V plot of p-type SLS TFTs measured at 100 kHz with source and drain grounded. The turn-on characteristics of C-V curves in the subthreshold region are similar to the I_{DS} versus V_{GS}

characteristics. This is because inversion of poly-Si TFT layer is accomplished by the injection of carriers from source and drain terminals, which is affected by the carrier transport in poly-Si films. Grain boundary traps affect the C-V characteristics by changing the surface potential at gate oxide/poly-Si interface, which will in turns affect semiconductor capacitance C_S and shows channel orientation dependent turn-on characteristics. The difference of C-V plots between parallel SLS TFTs and perpendicular SLS TFTs therefore can be used to extract the distribution of grain boundary trapped charge density D_{gb} by [5]

$$D_{gb} = \frac{1}{q}\left(C_{S,\perp} - C_{S,//}\right) = \frac{1}{q}\left(\frac{C_{ox}C_{meas,\perp}}{C_{ox} - C_{meas,\perp}} - \frac{C_{ox}C_{meas,//}}{C_{ox} - C_{meas,//}}\right)$$

where $C_{meas,\perp}$ and $C_{meas,//}$ are the measured capacitance of perpendicular SLS TFTs and parallel SLS TFTs, respectively. The calculated D_{gb} is about 2×10^{12} cm^{-2}-eV^{-1} as shown in the insert of Fig. 2.

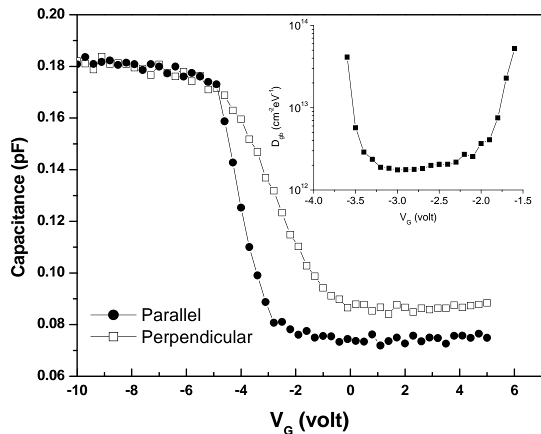

Fig. 2 Capacitance-voltage characteristics of p-type SLS TFTs. The C-V plots were measured at 100 kHz with source and drain grounded. The device dimension is W/L = 8 μm/6 μm.

(2). Gated-diode Measurements

Fig. 3 shows the reverse diode current I_R versus V_G of p-type SLS poly-Si gated-diode with different V_D when source floating. The I_R versus V_G curves shows the usual three distinct regions the same as MOS gated-diode [6]. The gated-diode is in off state when $V_G<V_{FB}$ and I_R originates from the generation-recombination centers in the depletion region of diffusion junction at drain end ($I_{gen,MJ}$).

When $V_{FB}<V_G<V_{th}$, the field induced junction is in depletion and the abrupt increase of I_R is due to the generation of electron-hole pairs at the field-induced junction depletion region ($I_{gen,FIJ}$) and the generation-recombination centers at gate oxide/poly-Si interface ($I_{gen,s}$). The $I_{gen,s}$ of p-type perpendicular and parallel SLS gated-diodes are about 20 pA and 17 pA, respectively. The $I_{gen,s}$ is independent of device channel length and V_D bias. The higher $I_{gen,s}$ for perpendicular SLS TFT than parallel SLS TFT is due to that there are more fine grain boundaries along channel direction in poly-Si film. $D_{it,}$ extracted from the $I_{gen,s}$ of gated-diode measurement for p-type perpendicular and parallel SLS TFTs are 3×10^{12} cm^{-2}-eV^{-1} and 1.7×10^{12} cm^{-2}-eV^{-1}, respectively.

At $V_G>V_{th}$, the field-induced junction is in inversion and I_R is reduced due to D_{it} filled by carriers supplied from drain contact. Both of $I_{gen,s}$ and $I_{gen,FIJ}$ are independent of device channel length, which implies the diffusion length of minority carriers is smaller than device channel length. Therefore, the channel is not fully depleted when V_D is small. The calculated depletion length is about 0.04 μm when trap density in poly-Si is 1×10^{18} cm^{-3}, which is smaller than the average width of a single fine grain 0.4 μm in SLS crystallized poly-Si film observed in SEM images. The gate voltage drops required to change the state of gated-diode from off to inversion when parallel SLS TFT and perpendicular SLS TFT biased at V_D = 0.1 V are about 0.9 V and 1.4 V, respectively. This turn-on voltage difference 0.5 V is independent of device type and V_D bias. Perpendicular SLS TFT has inferior turn-on characteristics than that of parallel SLS TFT because an extra 0.5 V is required to form inversion layer in the channel.

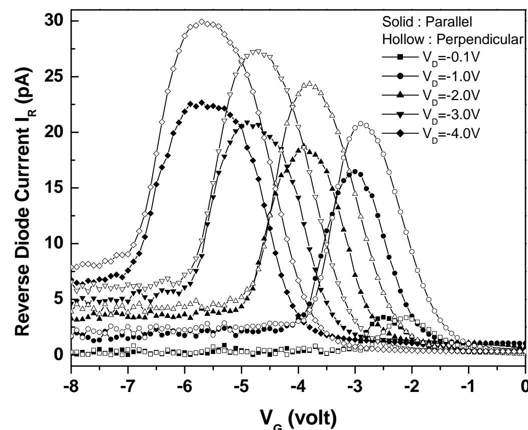

Fig. 3 The reverse diode current I_R of the gated-diode of p-type LTPS TFT is plotted as a function

of gate voltage V_G. The device dimension is W/L = 8 μm/4 μm

4. Summary

The channel orientation dependent turn-on characteristics of SLS poly-Si TFTs were studied by using gated-diode and C-V measurements. The grain boundary trapped charge density in poly-Si D_{gb} = 2×10^{12} cm^{-2}-eV^{-1} was extracted from the difference of C-V plots between parallel SLS TFTs and perpendicular SLS TFTs. The result of gated-diode measurement showed that perpendicular SLS TFT has inferior turn-on characteristics than that with parallel one, because more voltage drop was required to form inversion layer in the channel due to charge trapping at the grain boundaries. It was concluded that minimize the density of fine grain boundary is helpful to minimize the orientation dependent electrical characteristic of SLS poly-Si TFT.

5. References

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