Challenge to Future Displays: Transparent AM-OLED driven by PEALD grown ZnO TFT

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Abstract

We have fabricated 3.5" transparent AM-OLED panel driven by PEALD grown ZnO TFT. The performance of ZnO thin film transistor was improved by adapting top gate structure, protection layer for ZnO from photolithography process, optimizing temperature and plasma power of ZnO growth process. The ZnO-TFT has a mobility of 8.9 cm^2/V.s, a subthreshold swing of 0.95V, and an on/off ratio of 10^7.

1. Introduction

Since the reports for transparent amorphous oxide semiconductor thin film transistor (TFT) by Hosono group[1] and polycrystalline ZnO TFT by Wager group[2], oxide TFTs consisted of oxide semiconductor have attracted astonishing interests due to the applications for the display backplane such as organic light emitting diode (OLED)[3] and other electronics including ring oscillator.[4] Most of oxide TFTs have comprised sputtered zinc oxide, zinc tin oxide (ZTO), indium zinc oxide (IZO), or indium gallium zinc oxide (IGZO) and some of them have shown promising performance in terms of mobility and sub-threshold swing voltage (S.S).[5, 6]

Our group has developed transparent ZnO TFT array with mobility of about 1cm^2/V.s using atomic layer deposition (ALD) method for the application of OLED back plane.[7] Most of display researchers are reluctant to use ALD method due to the undeveloped large area equipment. Nevertheless, there are rather special attracts of ALD method for the oxide TFT process. First, ALD performed only by a surface reaction between precursors has been recognized as a unique fabrication technology by which high quality films with low structural imperfection can be obtained. One of the great merits in using ALD is low cost of precursor and no worry for the change of target that might happen during the sputtering process of oxide semiconductor. It has been suspected that oxide semiconductor target including zinc oxide becomes oxygen deficient as process proceeds. In addition, mobility around 3cm^2/V.s with high stability is enough to drive large area OLED. ALD grown ZnO-TFT can have that much of mobility.

The ZnO TFT by means of PEALD, however, have shown poor performance in the mobility and the hysterisis.[8] There could be many explanations for the poor performance, such as non ohmic contact between active and S/D electrode, damage of dielectric surface during the active layer process, non-optimized ZnO process, bottom gate bottom contact TFT structure causing interface contamination, or wet etching damage of ZnO layer, etc.

We have tried several processes of ZnO TFT to improve the TFT performance by means of PEALD. By adapting top gate structure and protection layer (PL) for ZnO from photolithography, and changing ZnO growth process, we obtained improved performance of PEALD grown ZnO TFT with high mobility, low S.S., and low hysterisis.

2. Experimental

For the film analysis, ZnO films were deposited on the sputtered SiO_2 coated glass substrate by means of PEALD at the substrate temperature of 150^oC using diethylzinc (DEZ) as Zn precursor and oxygen plasma as oxygen precursor at a plasma power of 60, 100, and 130W. The reactor pressure was 3 torr. In PEALD method, the precursors were alternatively injected into the reactor using Ar as a carrier gas with flow rate of 80 sccm. The pulsing times were 0.5 seconds for the DEZ, 1.5 seconds for oxygen plasma, and 2 seconds for Ar purge. The crystallographic orientation of the

ZnO films was determined by an x-ray diffractometer (XRD) with CuKα radiation. Surface roughness was measured by AFM.

For the fabrication of top gate TFT array, 100 nm thick SiO_2 coated glass was used for the substrate. After patterning of 150 nm ITO (S/D), 21nm thick ZnO semiconductor film was deposited by means of PEALD, followed by deposition of alumina, ZnO protection layer (PL). The active layer and PL were patterned by wet etching at once. The alumina (gate insulator) was deposited with the thickness of 160 nm at the temperature of 150°C by means of ALD, followed by S/D pad opening by wet etching of alumina. Sputtered ITO was used as gate and OLED anode and patterned by wet process. Fig. 1 illustrates the cross sectional view of unit TFT. For the integration of OLED, ZnO TFT array was coated with commercially available polymer dielectric material for the OLED anode bank process. The structure of transparent OLED grown by vacuum thermal deposition was 2-TNATA /NPD /Alq:C545T /Alq/LiF /Al/Ag and OLED encapsulation was carried out using glass.

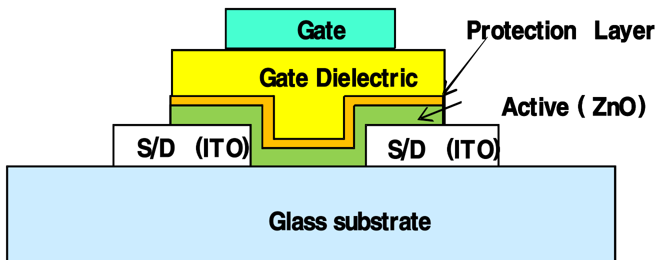


Fig. 1. Cross sectional view of top gate ZnO TFT with ZnO Protection Layer.

3. Results and discussion

We wanted to get rid of defects in the active layer by increasing the growth temperature. ZnO thin films grown at 150°C did not show any significant difference in surface SEM image and crystal orientation with the plasma power change as shown in the Fig. 2 and Fig.3.

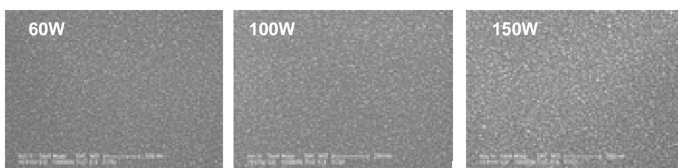


Fig. 2. SEM Images of ZnO films grown on the SiO_2 coated glass at various plasma powers.

On the contrary to the films grown at 100°C, the films mostly show (002) orientation.

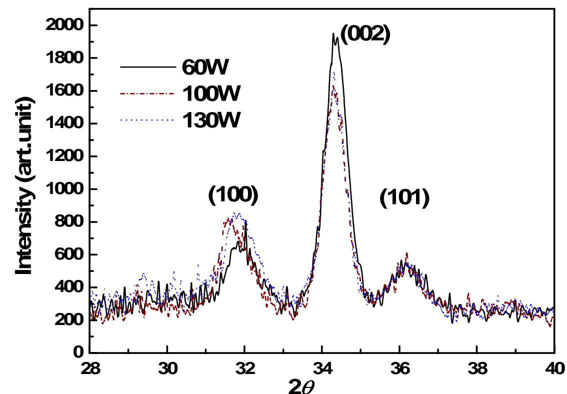


Fig. 3. XRD patterns of ZnO thin films deposited at various plasma powers at 150°C.

In the top gated structure, the flat surface roughness is important since surface itself acts the channel layer. We investigated surface morphology dependency of ZnO films on the plasma power by AFM and Table 1 summarized the results. Polycrystalline ZnO gave us rather rougher surface as the plasma power increased.

Table 1. Surface roughnesses of ZnO films grown at various plasma powers at 150°C.

Power (W)	Roughness (nm)	
	Rq (rms)	Ra (avg)
60	1.478	1.182
100	1.367	1.086
130	1.526	1.217

In a bottom gate structure of previous work[8], we could not obtain etching selectivity between the active layer and transparent conduction oxide (TCO) S/D. Thus, just bottom gate, bottom contact TFT was fabricated by wet etching process, in which channel is contaminated during lithography. Furthermore, when we used ALD grown ZnO:Al as an S/D electrode that can prevent dielectric surface damage during the deposition process of S/D electrode, we found serious contact resistance between PEALD grown ZnO active and ZnO:Al S/D. This drove us to adapt top gate TFT with ITO S/D as shown in Fig.1.

However, we had to be very careful in the selection of gate insulator in the top gate TFT, for most of gate insulators such as SiN_x, SiO_2 or alumina that are deposited on the active layer could make ZnO film conductive. The shallow donor level generated by

hydrogen or Al incorporation can be formed in ZnO during gate dielectric process. In addition, ZnO film can also become conductive depending on the following dielectric process temperature. With considering all these factors, we decided gate insulator material and process temperature not to increase carrier density in ZnO active layer. We also tried to optimize ZnO deposition condition by changing plasma power.

Although oxide TFTs consisted of SiN gate dielectric with excellent mobility had been reported[6], we concerned the inter-diffusion of oxygen in the interface. We adapted ALD grown alumina. Here, we lower the growth temperature to 150°C not to cause the Al incorporation into the ZnO layer, happening at high temperature process.

One thing very important in ZnO TFT is that ZnO is attacked even by weak base during photo-lithography. Especially our device has just 21nm thickness of ZnO, thus wet lithography process damage caused serious TFT performance degradation. This result led us to use protection layer (PL) for ZnO of alumina that covers ZnO just to protect from the patterning process as shown in Fig. 1. When choosing PL, we again had to be very careful not to make ZnO film conductive. The PL, alumina, was deposited by PEALD at 150°C with plasma power of 60 W.

Fig. 4 shows performance of ZnO TFTs fabricated at various plasma power of PEALD and table 2 summarizes the results. Although the AFM data showed rougher surface morphology as plasma power increased, the TFT showed rather improved performance with increasing plasma power. The mobility increased to 8.9 cm^2/V.s, V_{th} shifted higher, S.S decreased, and on/off ratio reduced. We are investigating other factors except surface roughness that can affect TFT performance.

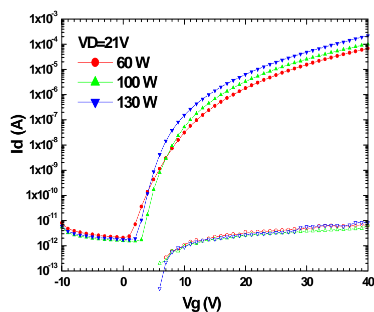


Fig. 4. Transfer characteristics of ZnO-TFT with W/L=40/10 at V_{DS} 21V fabricated at various plasma power.

Table 2. ZnO-TFT performance fabricated at various plasma power.

	60 W	100 W	130 W
mobility	2.47	3.3	8.9
S.S	1.43	1.0	0.95
on/off	3.2 x 10^7	6.7x 10^7	1.2 x 10^7

To drive OLED, reducing S.S is very important and we choose 130W process for the OLED backplane. As shown in the bottom gate ZnO TFT, the first measurement of top gate TFT induced kind of charge accumulation and it shifted $V_{turn\ on}$ positive direction.

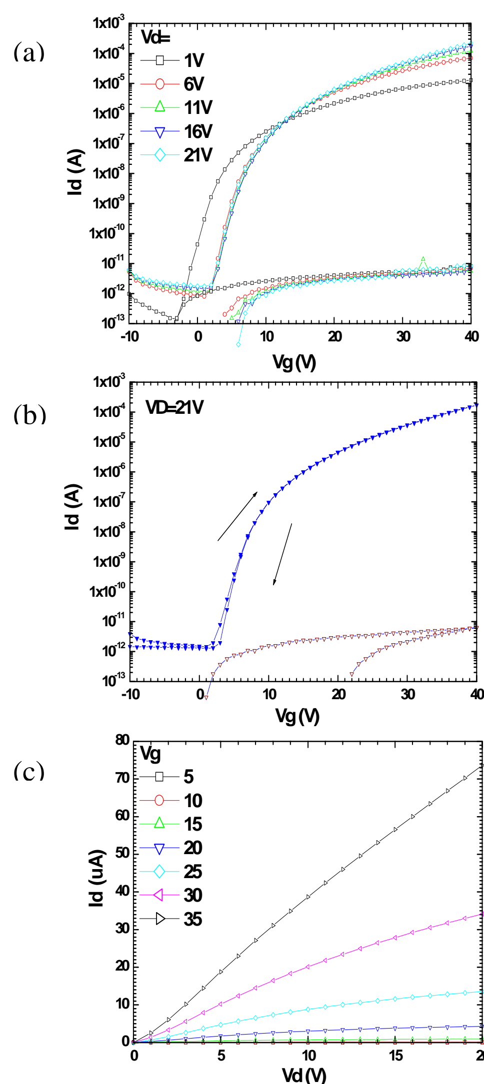


Fig. 5. Performance of ZnO-TFT grown at 130 W with a W/L=40/10 (a) Transfer characteristics for V_{DS} varying from 1 to 21V. (b) Hysterisis at V_{DS} 21V. (c) Output characteristics for V_{GS} varying from 5 to 35 V.

Fig. 5 shows ZnO TFT performance fabricated with plasma power of 130W. Hysterisis is samll, but it was very difficult to get hard saturation. Although we still see the contact resistance between the active and S/D electrode due to the increased ITO work function with the help of high oxidant of oxygen plasma, it was reduced by thermal annealing during following OLED integration process.

In a fabrication of transparent display, we know that the TCO conductivity is a big issue. It was very hard to drive OLED just with the commercialized ITO due to the IR drop. Thus we adapted ITO/Cr bi-layer for the data power line. Deposition of Cr on the just data power line decreased transmittance 20% as shown in Fig. 6.

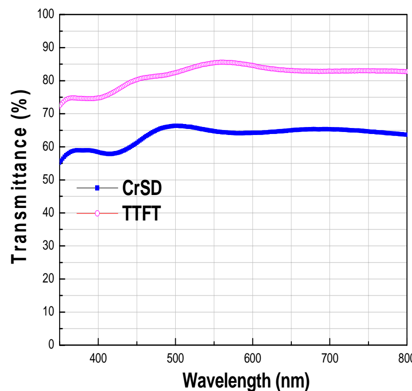
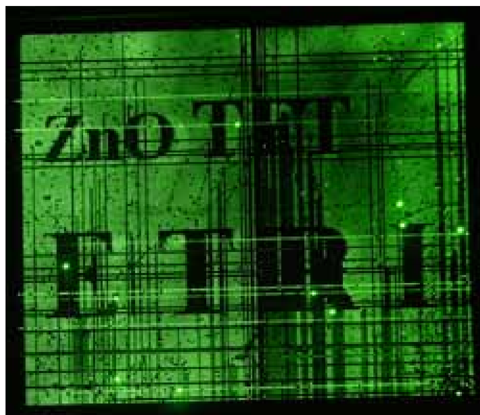


Fig. 6. Transmittance of ZnO TFT array



Panel size	3.5"
resolution	176 (scan) x 220 (data)
pixel pitch	312 x 312 μm^2

Fig. 7. Operation image of transparent AM-OLED driven by ZnO TFT.

Fig. 7 shows the transparent AM-OLED driven by ZnO-TFT. Now we are trying to search the way to improve panel performance such as panel structure, TFT performance, and TCO material properties.

4. Summary

We have developed 3.5 inch QCIF transparent ZnO TFT array and have integrated transparent OLED on the ZnO TFT backplane to fabricate transparent AM-OLED. The ZnO TFT performance could be improved by adjusting ZnO film process and adapting ZnO protection layer. Proper selection of gate insulator resulted in well behaved top gate ZnO TFT.

5. Acknowledgement

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