Nanotechnologies in Displays : TFTs with Carbon Nanotubes and Semiconductor Nanowires.

Didier Pribat[1], Costel Cojocaru[1], M. Gowtham[1], L. Eude[1], A. Balan[1], P. Bondavalli[2] and P. Legagneux[2]

[1]Ecole Polytechnique, Route de Saclay, 91128, Palaiseau Cedex.
TEL:+ 33 1 69333685, e-mail: didier.pribat@polytechnique.edu
[2] **Thales Research & Technology, 91767 Palaiseau, France**

Keywords : Carbon nanotubes, Semiconductor nanowires, Thin Film Transistors, Active Matrix Displays

Abstract

We propose new approaches to thin film transistor fabrication that use carbon nanotubes and semiconductor nanowires as active elements. These nanomaterials which are essentially studied in the context of the post CMOS era will certainly impact the active matrix display industry in the near future.

1. Introduction

The most mature, simple and cost effective thin film transistor (TFT) technology makes extensive use of hydrogenated amorphous silicon (a-Si:H). A simple figure stresses the importance of a-Si:H: about 150 millions of squared meters of glass substrates will be coated with this material in 2007, for the purpose of addressing active matrix liquid crystal displays (AMLCDs). However, due to some drawbacks, such as gate instabilities [1] (particularly when the duty cycle is high), other TFT technologies are currently needed and are been developed, especially for addressing organic light emitters (OLEDs) or for fabricating flexible displays. Low temperature polysilicon technology (LTPS) is one of those, but its acceptance in industry is still low, because it is complex [2] (and expensive) and its productivity (the throughput in particular) is lower than that achieved in AMLCD factories with a-Si:H.

Also, organic semiconductors and TFTs made of such materials [3] are currently being studied, but device stability might be an issue and standard materials and processing conditions are not in sight yet.

In this paper, we will present some new approaches to TFT fabrication (compatible with glass or even plastic substrates) that use popular nanomaterials, namely carbon nanotubes (CNTs) and semiconductor (essentially Si and Ge) nanowires (NWs). At this point, we also emphasise that carbon nanotube random networks can be used as transparent electrode material in replacement of ITO or ZnO-based materials.

CNTs and NWs can be grown or organised at low temperature and on non-crystalline substrates. As far as thin film transistors are concerned, the use of these nanomaterials could result in better characteristics (high mobility, low threshold voltage…) and above all, a very good stability. Hence, CNTs and Si or Ge NWs could become materials of choice for the addressing of organic light-emitting devices (OLEDs) in active matrix displays. Today, the major problem is to organise such nano-objects in a reproducible way, compatible with large scale manufacturing.

2. Carbon nanotubes

Single wall carbon nanotubes (SWNTs) can be viewed as resulting from rolling-up a graphene sheet into a seamless cylinder with a diameter between ~ 0.7 and several nanometers (nm). Depending on the way the C atoms connect when the cylinder is formed, SWNTs can be metallic or semiconductor [4]. For semiconductor specimens, the forbidden band gap is inversely proportional to the diameter d (Eg ~ 0.9 eV/d, with d expressed in nm). There is another category of CNTs, named multiwall carbon nanotubes

(MWNTs). These are made up of several concentric cylinders and they are metallic [4]. They are materials of choice for field emission devices [5].

Various synthesis methods are used for carbon nanotubes [6], with growth temperatures down to ~ 450°C for CVD-type methods [7]. However, as far as SWNTs are concerned, all these methods produce mixtures of metallic (m) and semiconductor (s) specimens (in principle, the m to s ratio is 1:2). Complex post-growth separation procedures have to be used [8] if one wants one type of SWNT only (metal or semiconductor). Moreover, SWNTs tend to group into bundles under the action of van der Waals forces, which complicates their separation. However, it has been shown that the m to s ratio was dependent on the synthesis method and for instance, 90% of s-type SWNTs have been obtained using a PE-CVD method [9].

Transistors made from *individual* s-type SWNTs are invariably p-type in air and they exhibit impressive properties, with hole mobility values of ~ 3000 cm^2/Vs, very low threshold voltages and subthreshold slope values of ~ 70 mV per decade of current [10]. Ballistic transport has also been demonstrated in short channel devices [11, 12]. The switching mechanism in these transistors is different from that of conventional CMOS devices, since carrier transport is controlled by Schottky barriers at the s-SWNT/metal contact [13]. As a consequence, p-type devices can transform to n-type transistors after annealing under vacuum [14], because the Fermi level alignment at the contacts (*i.e.*, the Schottky barrier height) is modified by the out-gasing of adsorbed oxygen molecules from the contact regions (see refs. 15 and 16 for recent reviews).

Devices made from *individual* s-SWNTs are usually prepared by spreading (typically by spin coating or dipping) a suspension of SWNTs onto a substrate, then indexing the position of specific specimens (by using scanning electron or atomic force microscopy) and subsequently performing e-beam lithography operations for the fabrication of the contacts. Controlling (or rather finding) the position and in-plane orientation of an individual SWNT is therefore a complicated task, which is not amenable to mass fabrication. Moreover, once a SWNT spotted on the substrate and contacted, its conductivity has to be measured in order to assess whether it is semiconducting or not. Finally, for semiconducting specimens, small variations in diameter (*ie.*, in the band gap) will induce irreproducibility in transistor characteristics.

As an alternative to the unrealistic process of using individual SWNTs for device fabrication, researchers have recently investigated the possible use of random CNT networks. When the SWNT coverage is high, random networks behave like conducting films (m-type SWNTs percolate and impose their transport properties), whereas at low coverage, a semiconducting behaviour is obtained, because only the s-SWNT form a percolating network. Recent studies show that the conductivity in the networks is controlled by the Schottky barriers at the contacts between metallic and semiconducting tubes [17]. In fact, random s-SWNT networks can be viewed as a polycrystalline semiconductor material, where individual tubes would replace grains; the grains would be separated by potential barriers and transport would take place according to a model similar to the well-known Seto model [18] for polycrystalline silicon.

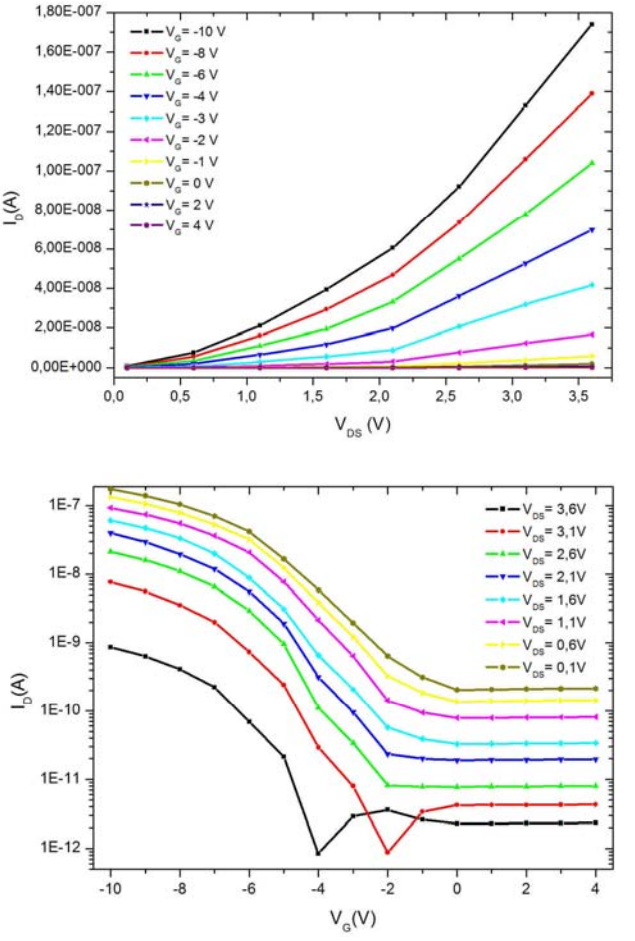

Fig. 1. Electrical properties of TFTs built with random CNT networks. Top: output characteristics. Bottom: transfer characteristics.

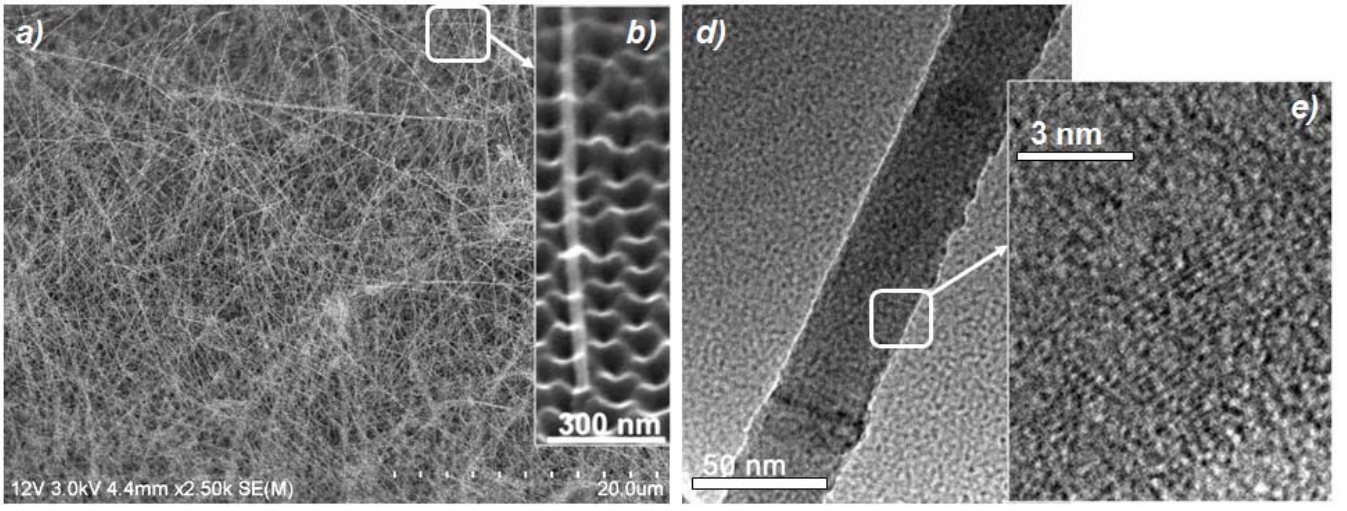

Figure 2: (a): Top view of Si nanowires grown in a vertical anodic alumina membrane. For easy observation, the growth time has been prolonged purposely, which results in NWs growing out of the membrane. (b): Close view of a nanowire emerging from a pore. (d) and (e): Transmission electron microscope views of a nanowire. Crystallographic planes can be observed on (e).

Accordingly, carrier mobility in devices made from random networks is lower than in the corresponding devices made from individual SWNTs. However, typical mobility values are around 10 cm^2/Vs and above [19], which is still better than most TFT technologies except LTPS.

Random networks are generally obtained by spraying, filtration, spin coating, etc… from a precursor suspension of SWNTs in a solvent. They yield reproducible electrical results because of the averaging of physical characteristics over a large number of SWNTs. However, the fabrication of CNT suspensions is by no means an easy task, since as grown SWNTs are not soluble in most solvents. In brief, after growth and purification (operations usually performed by the company selling CNTs), the SWNTs are mixed with the appropriate solvent (and surfactant), then they are sonicated, in order to break the bundles and yield individual SWNTs. The mixture is subsequently submitted to ultra-centrifugation in order to separate individual SWNTs from the remaining bundles and catalyst impurities. Finally, the supernatant is carefully recuperated.

Figure 1 presents some properties of bottom gate TFTs fabricated with random CNT networks in our lab. The on/off ratio is not so good because we have not yet optimised the preparation of the suspension and the deposition procedure. There are probably too many metallic tubes, which give rise to the high off-current. A simple method has been proposed in order to selectively burn metallic tubes [20], but because SWNTs always come in bundles (despite the sonication process), semiconductor specimens in a bundle are also destroyed or at least damaged [21]. The best compromise is probably to use SWNT mixtures with a high fraction of semiconductor specimens as can be obtained by PE-CVD [9] or by the CoMoCat process [22]. Also, using a bottom gate TFT structure is not ideal for a good coupling between the gate and the tubes [10]. In summary, random SWNT networks certainly have the potential to become a relevant TFT technology in the future.

3. Semiconductor nanowires

Semiconductor nanowires (NWs) from column IV are currently being extensively studied for the replacement of traditional CMOS devices. Si or Ge NWs are usually grown by the vapour-liquid-solid (VLS) technique (using *e.g.*, gold catalyst particles), which was developed 40 years ago for growing single crystals [23]. The VLS process (that can be tailored to be temperature-compatible with glass substrates) has recently been applied to the growth of NWs and high performance field effect transistors (made with individual NWs) have been demonstrated, exhibiting mobility values up to ~ 1300 cm^2/Vs [24].
The problem here again is to organise these NWs on the surface of a substrate, in order to control their

placement and in-plane organisation. Template growth in porous alumina [25, 26] is one way of organising nanowires. Figure 2 shows Si nanowires grown in a vertical alumina membrane using the gold-mediated VLS method. The diameter of the NWs is quite uniform due to the fact that the size of the gold catalysts is gauged by the pores of the alumina membrane.

We are currently developing a novel template-based method for the collective organisation of nanowires [26, 27]. This method makes extensive use of porous anodic alumina as a template material. However, the pores are synthesised parallel to the surface of the substrate (instead of perpendicular as usually done), which facilitates the contacting operations for a three terminal device (planar-type technology). Once the lateral template synthesised, the bottom of the pores can be filled with gold catalyst particles (using an electrodeposition process) and the VLS growth of Si NWs can subsequently be achieved inside the lateral pores. "Films" of Si NWs embedded in alumina membranes can then be processed just like classical thin films (lithography, etching …) and there is no need to manipulate individual NWs in order to organise them in a device. The process can be used to fabricate active matrix backplanes with a reduced number of masks [28].

4. Summary

We have reviewed some properties of carbon nanotube random networks and emphasised their possible use for TFT applications. We have also presented the organised growth of semiconductor (Si, Ge, ..) nanowires and suggested their interest for the fabrication of active matrix backplanes.

5. References

1. M.J. Powel, C. van Berkel, and J.R. Hughes, *Appl. Phys. Lett.,* **54**, 1323 (1989).
2. D. Pribat, *Proceedings of the third International Meeting on Information Displays (IMID)*, p. 50, 2003.
3. See *e.g.* : C.D. Dimitrakopoulos, and D.J. Mascaro, *IBM J. Res. Develop*., **45**, 11 (2001). C. Reese, M. Roberts, M-m. Ling, and Z. Bao, *Materials Today*, p. 20, September 2004. A. Dodabalapur, *Materials Today*, p. 24, April 2006.
4. "Physical Properties of Carbon Nanotubes", R. Saito, G. Dresselhaus, and M.S. Dresselhaus, Imperial College Press, 1998.
5. E. Minoux *et al*., *Nano Lett*., **5**, 2135 (2005).
6. A. Loiseau *et al*., in « Understanding Carbon Nanotubes », A. Loiseau, P. Launois, P. Petit, S. Roche and J.-P. Salvetat Eds., Springer Lecture Notes in Physics, Springer 2006, pp. 49-130.
7. Y-S. Min, E.J. Bae, B.S. Oh, D. Kang, and W. Park, *J. Am. Chem. Soc*., **127**, 12498 (2005).
8. R.C. Haddon, J. Sippel, A.G. Rinzler, and F. Papadimitrakopoulos, *MRS Bulletin*, p. 252, April 2004.
9. Y. Li *et al., Nano Lett.*, **4**, 317 (2004).
10. A. Javey *et al*., *Nature Materials*, **1**, 241 (2002). A. Javey *et al*., *Nano Lett.*, **4**, 447 (2004).
11. A. Javey, J. Guo, Q. Wang, M. Lundstrom and H. Dai, *Nature*, **424**, 654 (2003).
12. A. Javey, P. Qi, Q. Wang, and H. Dai, *Proc. Nat. Ac. Sci.,* **101**, 13408 (2004).
13. S. Heinze *et al*., *Phys. Rev. Lett.*, **89**, 106801 (2002).
14. V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, "Carbon nanotube inter and intra molecular logic gates", *Nano Lett.*, **1**, 453 (2001).
15. H. Dai, A. Javey, E. Pop, D. Mann, W. Kim and Y. Lu, *Nano*, **1**, 1 (2006).
16. Ph. Avouris and Jia Chen, *Materials Today*, p. 46, October 2006.
17. E. Bekyarova, M.E. Itkis, N. Cabrera, B. Zhao, A. Yu, J. Gao and R. Haddon, *J. Am. Chem. Soc*., **127**, 5990 (2005).
18. J.Y. Seto, J. Appl. Phys., **46**, 5247 (1975).
19. E. Snow, J.P. Novak, P.M. Campbell and D. Park, *Appl. Phys. Lett*., **82**, 2145 (2003).
20. P.C. Collins *et al., Science*, **292**, 706 (2001).
21. R. Seidel *et al*., *Nano Lett*., **4**, 831 (2004).
22. G. Lolli, L. Zhang, L. Balzano, N. Sakulchaicharoen, Y. Tan and D. Resasco, *J. Phys. Chem.,* **B 110**, 2108 (2006).
23. R.S. Wagner, in "Whisker technology", Wiley, p. 47, 1970.
24. Y. Cui *et al*., *Nano Lett.*, **3**, 149 (2003).
25. redwing
26. D. Pribat, C. Cojocaru, and A. Rumyantseva, Proceedings of the 1rst International TFT Conference (ITC 2005), p. 160, 2005.
27. C. Cojocaru *et al*., *Nano Lett*., **5**, 675 (2005).
28. D. Pribat, C. Cojocaru, M. Gowtham, L. Eude, P. Bondavalli and P. Legagneux, accepted for publication in the *J. Soc. Inf. Displays*.