Study on operation stability of printed organic TFTs

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Abstract

We have been developing printed organic TFTs for flexible displays. In this study, we have pay attention to the operation stability improvement of the organic TFTs, and studied several factors especially depending on the dielectric layers. From the detailed analysis of the effects of dielectric layers, we have proposed a new printed dielectric layer which is mainly consisting of metal oxide and gives high operation stability

1. Introduction

It has been recognized that organic TFTs are one of the most promising TFTs for flexible displays. They are suitable for flexible devices due to the plasticity of the materials. It can be prepared by printing techniques at relatively low temperature. Therefore, it can be easily prepared on a plastic substrate directly without any process damages on the substrate. In recent years, the development of the organic TFT has accomplished remarkable progress. Even in the organic TFTs prepared by printing process, high field effect mobility came to be obtained.

On the other hand, improvement of reliability has become important for practical use of organic TFTs. Especially, control of threshold voltage (V_{th}) is one of the most important issues to improve TFT stability. It has been known that V_{th} strongly depends on a property of the gate dielectric such as capacitances of gate dielectrics, traps at dielectric/semiconductor interfaces and so on. We have been developing printed organic TFTs for displays [1].

In this paper, we introduce several preparation techniques using solution process of organic TFTs to show high TFT performance. Furthermore, factors that govern the stability of the device operation are also discussed. Especially, we have examined influence of quality of the gate dielectric on V_{th}, and are going to suggest suitable gate dielectric layer condition to the organic TFTs.

2. Thin film preparation of an organic semiconductor

Control of the organic semiconductor film quality is one of the most important technologies to obtain a high performance organic TFTs. Promising film preparation conditions by a print method are different with each organic semiconductor. We have examined several printing techniques of the organic semiconductor layer, and found that the control of the crystallization point in the spread solution on a substrate is essential to give an organic thin film with high quality for transistors. In case of small molecules, deposition speed, ink temperature, and surface energy of a substrate are important to control the film quality.

Figure 1 shows pentacene thin films prepared by solution process. Film (A) was prepared by highly temperature controlled solution process. Film (B) was roughly prepared by solution process. It is clear that the film (A) has higher quality. The quality of the film was also superior to the vacuum deposited film. Mobility of the film (A) was found to be ca. 1cm^2/Vs. This is the largest level as the printed organic TFT.

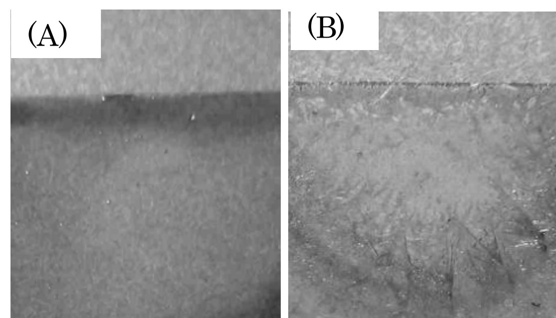

Fig.1. Pentacene thin films deposited by the solution process.

3. Stability analysis of device operation

We have investigated several factors for TFT stabilities such as V_{th} shifts. Figure 2 shows dependence of V_{th} on gate capacitance. V_{th} was proportional to the reciprocal of gate capacitance. Furthermore, large capacitance gave large fluctuation of V_{th}. Average fluctuation of Vth for the pentacene TFT with 1000 nm SiO_2 gate dielectric was approximately 5V, however it became only 0.5 V for the TFT with a 100 nm-SiO_2 dielectric layer. This reduction of fluctuation would be attributed to the charge fluctuations (ΔQ) at the pentacene/SiO_2 interface that is converted to voltage fluctuations of $\Delta Q/C$. The voltage fluctuation reduces with increase in capacitance. These results suggest that effects of enhancement of the gate capacitance are not only lowering threshold voltage but also reducing fluctuation of V_{th}.

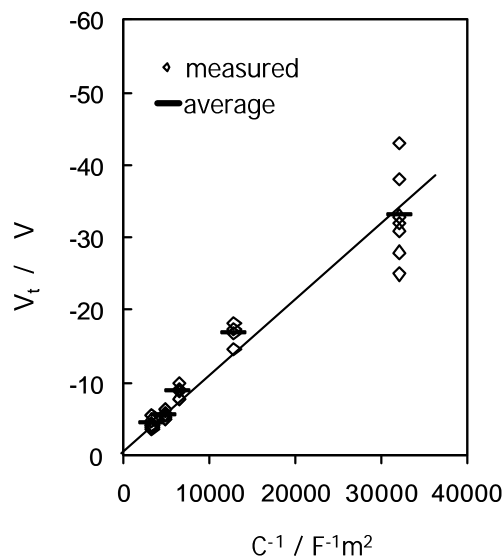

Fig. 2. Dependence of V_{th} on capacitance

We have also investigated an effect of surface condition on V_{th} shift for pentacene TFT with a SiO_2 gate dielectric. At the beginning, the effect of SAM treatment on the SiO_2 dielectric layer was investigated. Several kinds of SAM layer with different alkyl chain lengths were coated on a SiO_2 dielectric layer for pentacene TFTs. Figure 3 shows the V_{th} shift for pentacene TFTs with several SAM layer on the SiO_2 gate dielectric. From the figure, it can be recognized that the SAM with longer alkyl chain gave larger V_{th} shift for the pentacene FET. Furthermore, it was revealed that the main origin of the V_{th} shift came from carrier traps from the temperature dependence study of the V_{th} shift. These results mean that existence of alkyl chain at the gate dielectric/organic semiconductor interface increase the trap density and reduce the TFT stability.

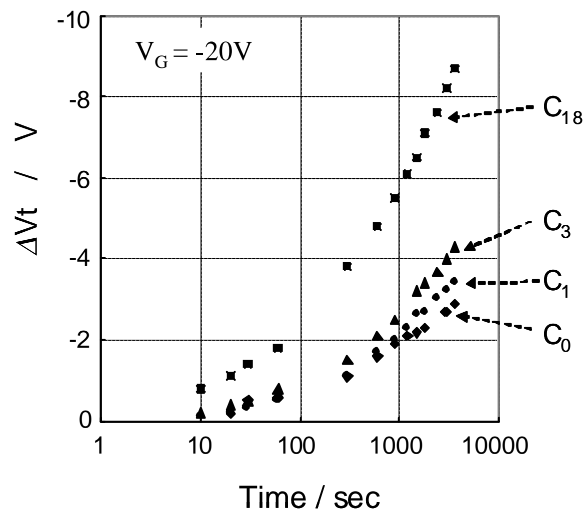

Fig.3. V_{th} shifts for pentacene TFTs with several SAM layer on the SiO_2 gate dielectric.

The effect of surface roughness of the gate dielectric layer on the Vth shift was also examined for pentacene TFTs. In figure 4, V_{th} shift after 2000 sec bias stressed was plotted against the RMS value of the SiO_2 gate dielectric layer of pentacene TFTs. The figure suggests that the surface roughness is very sensitive to the V_{th} shift.

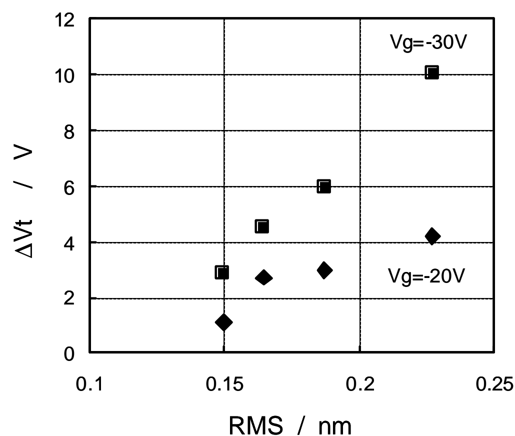

Fig.4. Dependence of V_{th} on surface flatness.

From these results, we have found that few alkyl components at the organic semiconductor and gate dielectric layer interface give stable device operation for the organic TFTs. This result suggests that a conventional polymer gate dielectric layer is not suitable for the organic TFT to give stable device operation.

4. Printed gate dielectrics for organic TFTs

As mentioned above, it is very important to develop a printing technique for all components of the printed TFTs which is suitable to keep the reliability. Therefore, we have also developed a new technique to prepare a metal oxide layer with enough high dielectric properties as a gate dielectric layer by printing method [2]. We have employed UV-ozone oxidization reaction of precursor compounds.

Here, a preparation technique to give a SiO_2 dielectric layer with high dielectric properties by solution process. A silazane compound was used as a precursor material. It was dissolved in an adequate solution, and spread on a solid substrate by spin coating technique. The coated film was heated about 150 °C to vaporize the solvent. After the vaporization of the solvent, the film was annealed at successive step-wise temperature under UV-light irradiation. UV light was irradiated to assist the ozone oxidization reaction. By investigating several preparation conditions, we have succeeded in preparation of a SiO_2 film with high dielectric properties by low temperature solution process. Especially, the process temperature could be down to below 200 °C. Therefore, it is possible to prepare the SiO_2 dielectric layer on a PET film.

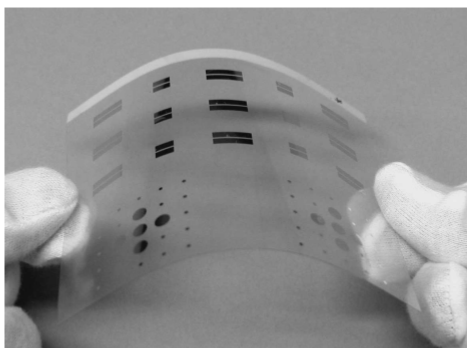

Fig.5. SiO_2 film converted from silazane prepared on a PET film

The prepared film surface was extremely flat. The radius of mean-square (RMS) values of the SiO_2 film was estimated to be 0.15 nm by the AFM measurement. As a conventional solution process of a SiO_2 film preparation, Sol-Gel technique is a popular and good candidate. However, it has been known that it is not easy to prepare such a flat surface of the SiO_2 film by the Sol-Gel technique. Structural properties of prepared SiO_2 film in this work were almost same among the precursor materials used in this study.

Dielectric property of the prepared SiO_2 film was estimated by *J-E* measurements. Figure 4 shows the leakage current density depending on the applied electric field for the prepared SiO_2 film. Up to 6 MV/cm of the applied electric field, the resistivity was almost constant in the order of 10^{15} Ωcm. Sharp break down phenomenon could be observed at 6 MV/cm indicating that its dielectric strength is ca. 6 MV/cm.

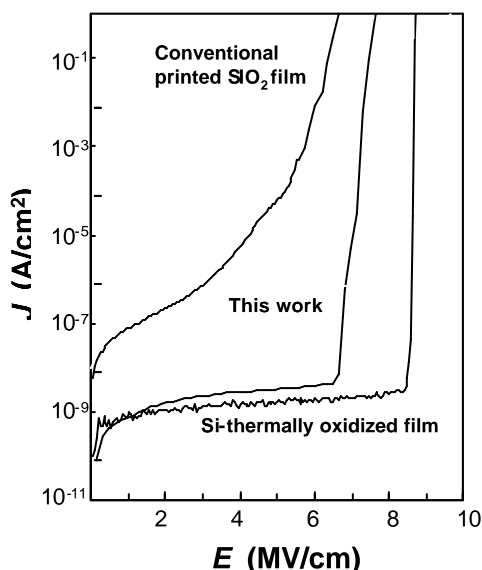

Fig.6. *J-E* characteristics for SiO_2 thin films.

In order to estimate the prepared SiO_2 film quality, dielectric properties were compared among SiO_2 films prepared by various deposition techniques. The parameters are listed in Table 1. As for surface morphology, SiO_2 thin film fabricated by thermal oxidation has extremely smooth surface, though the surface of SiO_2 thin films prepared by CVD and sol-gel technique have a poor smoothness. On the other hand, it was found that the solution processed SiO_2 thin film showed the very smooth surface of a same level as the SiO_2 film prepared by thermal oxidation.

The resistivity of our developed solution processed SiO_2 thin film was estimated to be the order of 10^{15} Ωcm. The breakdown was not found until the electric field of 6 MV/cm. The resistivity of SiO_2 thin films fabricated by thermal oxidation and sputtering technique were estimated to be the order of $10^{14} – 10^{15}$ Ωcm and dielectric strength was ca. 8 MV/cm. Therefore, it can be said that the newly developed solution process in this study gives a SiO_2 film of which dielectric properties are almost comparable to the thermally oxidized film even though it maximum process temperature is below 200 °C. As references, dielectric parameters for SiO_2 films prepared by different techniques are listed in Table 1. The resistivity and dielectric strength of SiO_2 thin film prepared by CVD technique was estimated to be order of 10^{13} Ωcm and 10 MV/cm, respectively. Dielectric property of the SiO_2 film prepared by a sol-gel technique was very poor. Its resistivity was order of 10^{10} Ωcm and dielectric strength was below 3.5 MV/cm. These results indicate that the solution processed SiO_2 thin film reported in this study is much suitable for the fabrication of SiO_2 gate dielectric for the printing technique.

TABLE 1. Preparation temperature, surface rough ness and dielectric properties of several SiO_2 thin fi lms prepared by various techniques.Periodic table of elements

Preparation Method	Temp. (°C)	RMS (nm)	Resistivity (ohm ·cm)	Dielectric Strength (MV/cm)
Thermal Oxidation	950	0.139	10^{14}~ 10^{15}	~8
Sputter	300	0.172	10^{14}~ 10^{15}	~10
Thermal CVD	900	0.916	~10^{13}	>10
Sol-gel	500	0.921	~10^{10}	~3.5
Solution Process (This Work)	200	0.152	~10^{15}	~6

This newly developed printing technique of a metal oxide layer is quite useful to prepare a gate dielectric of the printed organic FET which shows high operation stability.

5. Summary

We have developed printing techniques for preparing parts of organic TFTs. By applying these techniques, we have tried to prepare an organic TFT arrays for flat panel displays. The prepared arrays showed very high performance for the display drive. It indicates that our developed techniques are preferable to give its high performance.

6. Acknowledgements

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7. References

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