Low cost energy recovery circuit for PDP using Planar Transformer networks

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abstract

A new planar transformer type energy recovery circuit for PDP is proposed in this paper. The same current is transferred through both the primary and secondary sides during the energy recovery period. The conduction loss is reduced. Fabrication through simple manufacturing processes is possible using the PCB winding.

1. Introduction

Plasma display panels (PDP) come into the spotlight due to high contrast ratio, large screen size, wide viewing angle and rapid response time. The physical structure of the AC-PDP brings about inherent capacitive characteristics, and thus it requires an AC-voltage source with soft transition [1-2]. During the sustain period, the number of sustain pulses determines not only the contrast ratio but also total energy loss. There exist several researches focused on the high energy recovery (ER) efficiency, low device stress, EMI reduction and cost reduction. The current injection mode [3] achieved full zero voltage switching (ZVS) of the main switches and low EMI, but the higher current stress resulted in higher conduction loss. The current compensation method [4] accomplishes higher efficiency, but the injected current leads to lower efficiency during the display off mode. Though the inductive current source type [5] has a simple structure and multiple functions, the circulating loss and hard switching causes lower efficiency. The multi-level sustainer [6] reduces the voltage and current stress, but it has a high cost due to a larger number of devices.

Recently, the transformer based magnetic coupled energy recovery circuits (ERC) were researched [7-9]. A transformer is utilized instead of the capacitive resonant source and the number of devices is reduced using the leakage inductance and body diode of the switches.

In this paper, a new transformer based ERC is proposed. Using the panel voltage, the energy is recovered not to the capacitor but to the source. The resonant current flows through both the primary and secondary side of the transformer, and hence it reduces the conduction loss. Printed circuit board (PCB) winding and a low profile (LP) type core is utilized to the transformer design for the feasibility of mass production. The proposed mechanism is verified with a 42-inch PDP prototype.

2. Mode Analysis

Figure 1 shows the proposed ERC. It is composed of 4-main switches, 4-auxiliary switches, 4-auxiliary diodes and two transformers. The leakage inductance of each transformer is used for the resonant inductor. The body diodes of the main and auxiliary switches are substituted for the clamping diodes. During the transition, once the current starts to flow to the primary side of the transformer, the panel voltage is applied to the secondary side of the transformer and reflected to the primary side. Using the difference between the source and panel voltages, the leakage inductor resonates with the panel capacitance, and thus the energy is recovered to the source voltage. Figure 2 shows the operational waveforms of the proposed ERC. For simplicity in understanding the proposed scheme, the switches and diodes are assumed

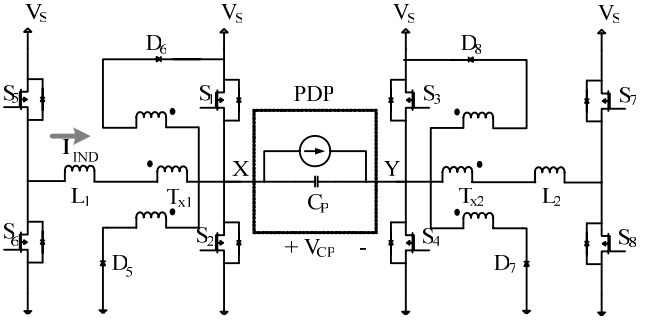


Fig. 1. Proposed ERC

to be ideal here. Since the operation of the two half cycles is symmetric, mode analysis is performed only for the first half cycle. The detailed mode by mode analysis is as follows.

Mode 1 (t_0-t_1) : At t_0, S_5 conducts and mode 1 begins. The panel voltage is applied to the secondary side of the transformer (T_{X1}), and thus the total voltage source for the resonance is (V_S-(n+1)V_{CP}). L_1 resonates with C_P until V_{CP} goes to V_S. Half of I_{CP} flows through the primary side and the remaining I_{CP} flows through the secondary side of the transformer.

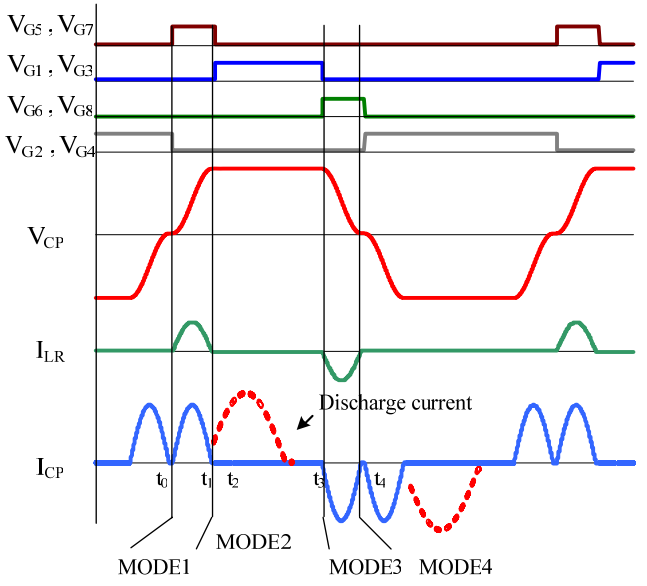


Fig. 2. Key waveforms

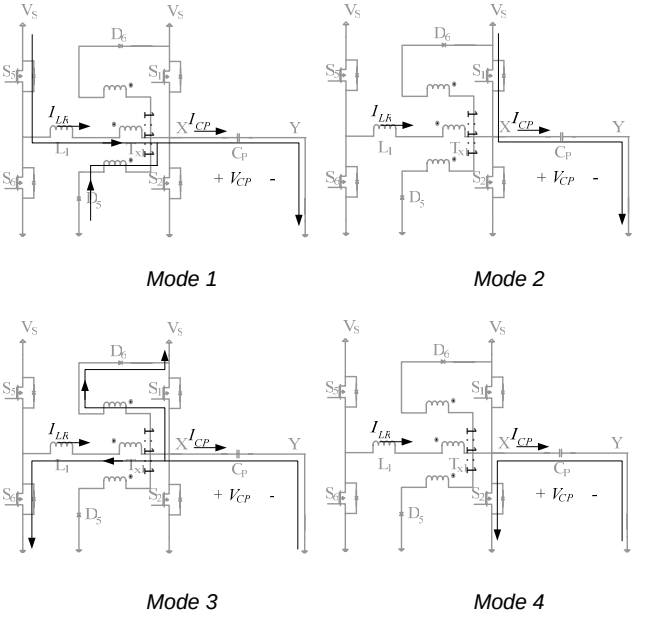


Fig. 3. Equivalent circuit diagram in each mode

$$v_{CP}(t) = (V_S - (n+1)V_{CP})\cos(n+1)w_0 t + I_0\sqrt{\frac{L_1}{C_P}}\sin(n+1)w_0 t \quad (1)$$

where $\omega_0 = \frac{1}{\sqrt{L_1 C_p}}$, I_o = initial current

Mode 2 (t_1-t_3) : After V_{CP} goes to V_S at t_1, S_1 turns on. The panel starts to discharge and the panel voltage is held by V_S. The remaining inductor current is recovered to V_S. At t_2, the inductor current is zero, and SXR is turned off with zero current switching. The panel continues to discharge.

Mode 3 (t_3-t_4) : After the panel discharges, the stored energy in the panel begins to recover. Once the current starts to flow, V_{CP} is applied to the tertiary winding, and thus L_1 starts to resonate with C_P and the panel voltage goes to zero. Half of I_{CP} flows through the primary winding and the remaining I_{CP} flows through the tertiary winding of the transformer.

Mode 4 (t_4-) : The panel voltage goes to zero and S_2 turns on with ZVS. The next half cycle begins.

In Equation (1), there exists design flexibility through the use of the transformer. The portion of the current which flows through either the primary side or the secondary side (or tertiary side) of the transformer can be controlled by the turns ratio (n). Through the consideration of higher efficiency, a turns ratio close to 1:1 is desirable.

3. PCB transformer

To utilize the leakage inductance and insure the uniform parameters of the transformer, the PCB transformer is one of the best techniques. The board patterns can be utilized for the winding. Moreover the LP type core expends the equivalent cross-sectional area of the transformers, which reduces the winding turns for the required power handling capability. In the ER circuit, the conduction time (D) of the auxiliary switches is very short, and hence the size of the transformer can be small. The key design equation for the transformer optimized for the PDP driving sequence is described in (2).

$$v_{rms} = \sqrt{\frac{1}{T}\int_0^{DT}\left(\frac{V_P}{2}\right)^2 (1-\cos wt)^2 dt} = \frac{V_P}{2}\sqrt{\frac{3D}{2}}$$

$$i_{rms} = \sqrt{\frac{1}{T}\int_0^{DT} I_P^2 \sin^2 wtdt} = I_P\sqrt{\frac{D}{2}}$$

$$P_t = V_{rms} \times I_{rms} = \frac{V_P I_P}{4}\sqrt{3}D$$

$$K_g = \frac{P_t}{2K_e\alpha} = \frac{W_a A_c^2 K_u}{MLT}[cm^5] \qquad (2)$$

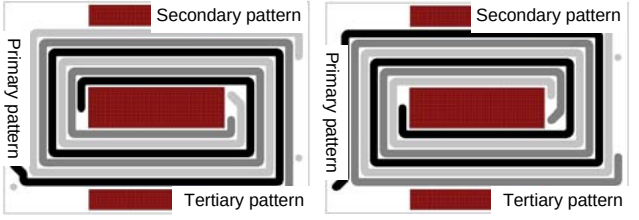
where $w = \frac{\pi}{DT}$, D = duty cycle

W_a : window area[cm^2], MLT : mean length turn [cm],

A_c : effective cross section of the core [cm^2],

K_u : window utilization factor $A_w^{'} / A_w \approx 0.1$

In case of PCB transformer, K_u is normally smaller then that of wire transformer due to the insulation and board layer thickness. With the same core volume, it results in more temperature rise. Using the interwinding PCB pattern as shown in Fig. 4, the proximity effect and the skin effect are minimized, hence the AC conduction loss is reduced.



(a) top layer (b) bottom layer

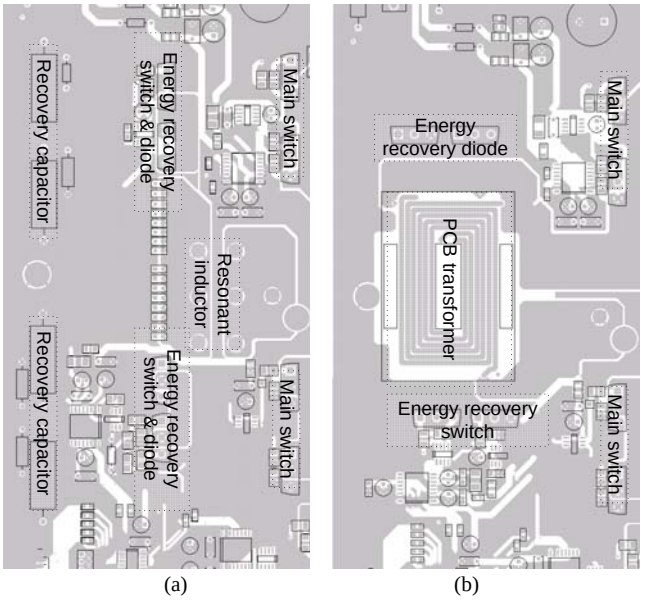
Fig. 4. PCB pattern schematics on each layer

4. Experimental Results

Using (2), the parameters of the transformer and devices are as shown in Table 1. Figure 5 shows the PCB layout of the previous version as well as that of the proposed version. Four capacitors for the energy recovery tank are replaced by a single transformer and the clamping diodes are removed. Figure 6(a) and (b) show the V_{DS_S2}, V_{DS_S4} and I_{L1} waveforms. it can be seen in Fig. 5(b) that the resonant current, I_{L1}, is reduced by 50%. Full ZVS is obtained in Fig. 6(d). Using the LP transformer, the energy recovery efficiency is lower than that of the normal transformer network. Two layers are not enough for the resistance of the winding, and thus it requires smart pattern layout in order to reduce the AC-resistance. With consideration of cost, there exists a tradeoff between the wide pattern and the multi-layer PCB.

TABLE 1. design parameters

Switch (S)	IXFK62N25
Diode (D)	FMB36S
Transformer (T_X,T_Y)	Core : PEE4319 (Samwha Co.) Bobbin : none Winding : PCB pattern (w:1.7mm, 4turns each, 2layers)
V_S	180V
fs	200kHz
Panel	42inch SD prototype



(a) (b)

Fig. 5. Board layout comparison; (a) previous version, (b) proposed version

5. Conclusion

In this paper, a new transformer type ERC is proposed. Using the panel voltage with the transformer turns ratio, full ZVS operation is achieved. The clamping diodes are removed and the conduction loss is decreased, thus allowing for additional cost reduction. The PCB transformer makes possible low cost mass production of the transformer type ERC.

6. Acknowledgements

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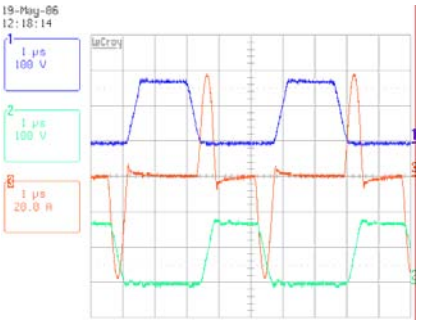
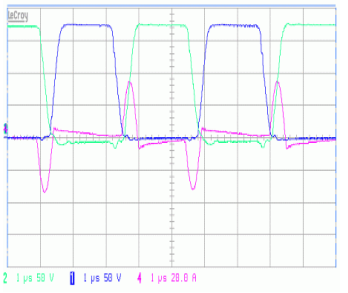
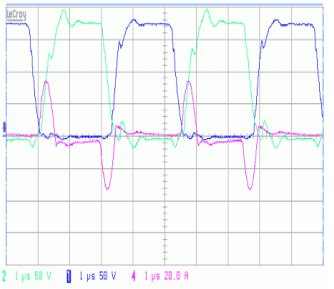


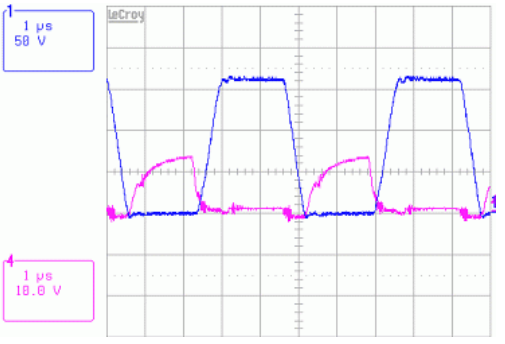
(a) previous version(black)



(b) proposed version (black),



(c) proposed version (white)



(d) ZVS operation of main switch (S_{XS}).

Fig. 6. key waveforms comparison;

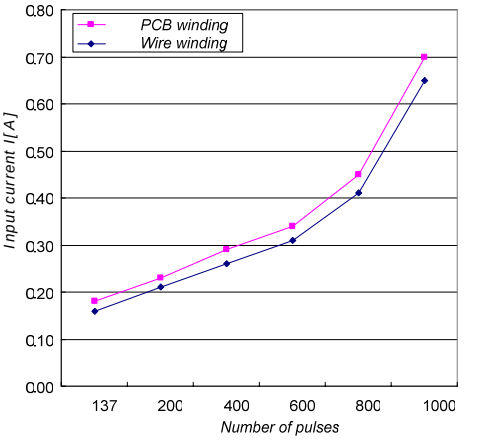


Fig. 6. I_{in} comparison w.r.t. the # of turns

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