Study on Discharge Characteristics Using V_t Close-Curve Analysis in ac PDPs

Byung-Gwon Cho and Heung-Sik Tae
School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, 702-701, Korea
TEL:82-53-950-6563, e-mail: hstae@ee.knu.ac.kr.

Keywords: AC PDP, Plasma Display, V_t close-curve, discharge characteristics, driving method

Abstract

The address discharge characteristics by the various scan-low and common-bias voltages are investigated based on measured address discharge time lags and V_t close-curve analysis. The scan-low voltages are changed under the same voltage difference between the X and Y electrodes during an address period. As the voltage difference between the scan and address electrodes is increased during an address period, the address discharge time lag is shortened but the background luminance is increased. It is found that the improved address discharge characteristics is caused by the effect of the higher external applied voltage during an address period than the accumulated wall charges during a reset period and the high background luminance can be prevented by applying an address-bias voltage during a rising-ramp period and low reset voltage.

1. Introduction

Plasma display panels (PDPs) have been one of the most promising large areas over 40-in. flat panel device suitable for high definition digital televisions. To compete with the other displays in a large size area, however, the cost reduction of the driving circuits in the present ac-PDP with three electrodes must be realized. One of the best methods for reducing a cost is to shorten the address time for the single scan driving and to lower the address voltage, thereby considerably lowering the cost of the address driving circuit. Though an address display-period separation (ADS) driving scheme has been considered to be the most stable driving method in the current ac-PDP [1], the long address time during an address period is still a critical issue to be solved for a high quality ac-PDP. For the realization of a high definition (HD) PDP by adopting the single scan method with a large area over 40-in., an address pulse width should be shortened under the low address voltage condition [2]. The long address time is fundamentally related to the formative and statistical time lags when applying the scan and address pulses during an address period [3]. Previous studies are focused on reducing the formative and statistical time lags, but the effects of the changes in the scan-low and common-bias voltages on the address discharge characteristics was not discussed.

In this study, the address discharge characteristics including the formative and statistical time lags by applying the various scan-low voltages are investigated based on the measured IR emission and V_t close-curve analysis. In addition, the reset discharge characteristics are also discussed in terms of a background luminance and IR waveform.

2. Discharge Characteristics

Fig. 1 shows the driving waveforms with various scan-low and common-bias voltages under the same voltage difference between the X and Y electrodes during an address period. The driving waveforms of Fig. 1 are applied to the 6-in. test PDP with a Ne-Xe (7 %) gas mixture. In Fig. 1, the V_{scl} means a scan-low voltage applied to the Y electrode, whereas the V_b means a common-bias voltage applied to the X electrode during an address period. The scan-low voltages during a reset and address period are set to the same voltage level. The initial applied voltages are given as follows: the scan-low voltage of 0 V and the common-bias voltage of 200 V, and the final applied voltages are the scan-low voltage of -200 V and the common-bias voltage of 0 V. The other driving conditions are V_{set} (reset voltage) of 210 V, V_s (sustain voltage) of 180 V, and V_a (address voltage) of 60 V. The scan-low voltage is decreased from 0 to -200 V,

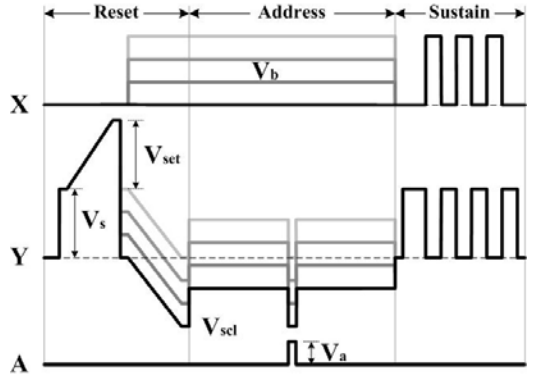

Fig. 1. Driving waveform with various scan-low and common-bias voltages by applying same voltage difference between X and Y electrodes during address period in this study.

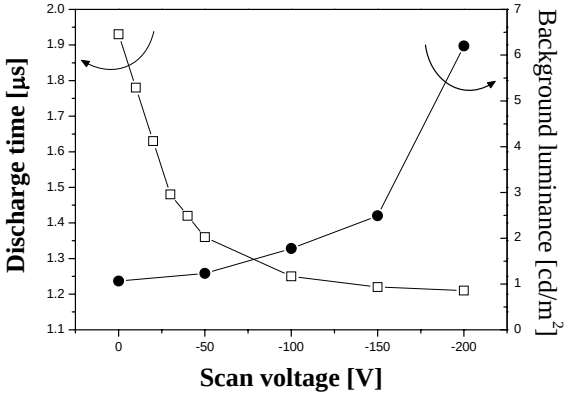

Fig. 2. Changes in address discharge time lags and background luminance with decrease in scan-low voltage.

whereas the common-bias voltage is decreased from 200 to 0 V at an interval of 50 V. The voltage difference between the common-bias voltage, V_b and the scan-low voltage remains constant at 200 V during an address period. The address discharge time lags are measured when the scan-low and the common-bias voltages are changed with the same voltage difference, as shown in Fig. 2. As the scan-low voltage is decreased, the address discharge time lag is shortened and has a tendency of the saturation.

The background luminance and reset discharge characteristics are investigated with a decrease in various scan-low voltages from 0 to -200 V in the case of the off-cell condition, as shown in Figs. 2 and 3. As the scan-low voltage applied to the Y electrode is decreased, the background luminance and the amount of IR waveform are increased because the plate-gap discharge between the Y and A electrodes are much produced by low falling-ramp voltage. In Fig. 3, when

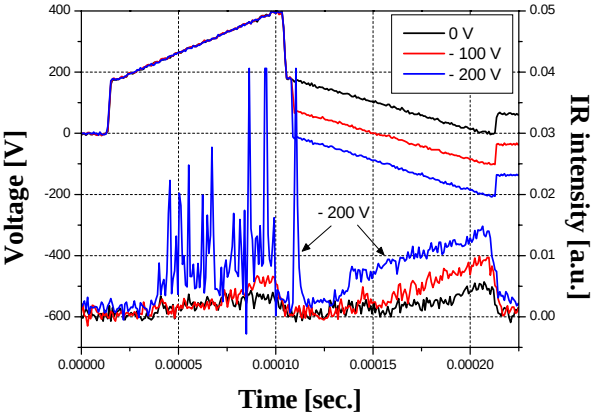

Fig. 3. Reset and corresponding IR emission waveforms with various scan-low and common-bias voltages during reset period.

the scan-low voltage during a reset period is applied at -200 V, it is found that the unstable reset discharge is produced during a rising-ramp period.

3. V_t Close-curve Analysis

Fig. 4 (a) shows the V_t close-curves on the applied voltage plane measured from the 6-in. test panel before applying the driving waveform. The horizontal axis indicates the threshold voltage between the X and Y electrodes, whereas the vertical axis indicates the threshold voltage between the Y and A electrodes. The typical V_t close-curve shape in the conventional panel structure is a hexagon with six sides indicating the threshold voltage, as shown in Fig. 4 (a). Thus the inner region of the V_t close-curve in Fig. 4 (a) means a non-discharge region, while the outer region means a discharge region [4].

Fig. 4 (b) shows the three different V_t close-curves on the applied voltage plane measured after a reset period when applying three driving waveforms with the scan-low voltage applied to the Y electrode of 0, -100, and -200 V in Fig. 1. The corresponding bias voltages applied to the X electrode are changed to 200, 100, and 0 V, respectively. Fig. 4 (b) indicates that the wall voltage between the X and Y electrodes are redistributed to the same amount irrespective of the types of the driving waveforms because the voltage difference between the X and Y electrodes during a reset period is the same as the conventional case. However, the wall voltage distribution between the Y and A electrodes are changed considerably depending on the scan-low voltages applied to the Y electrode. That is, for the case of the scan-low voltage of 0 and -

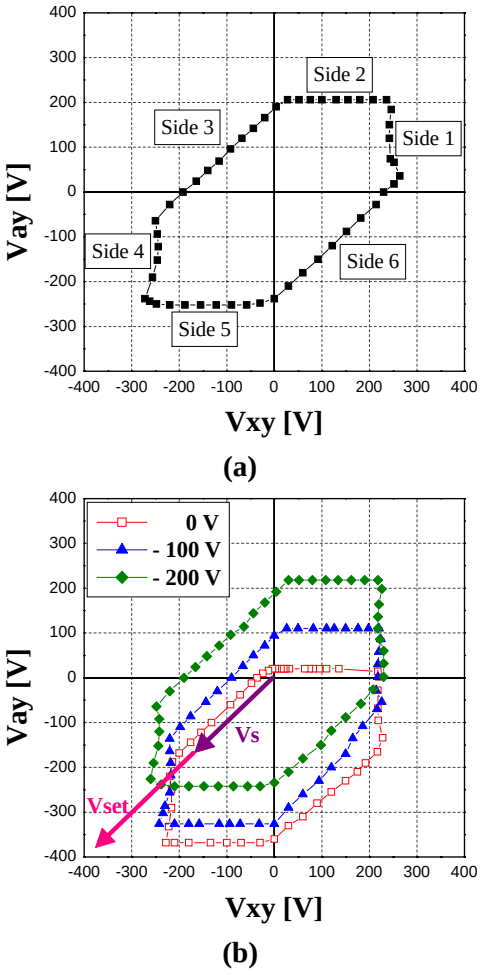

Fig. 4. Measured V_t close-curve on applied voltage plane (a) before applying driving waveform and (b) after reset period when applying driving waveforms with reset voltage vectors.

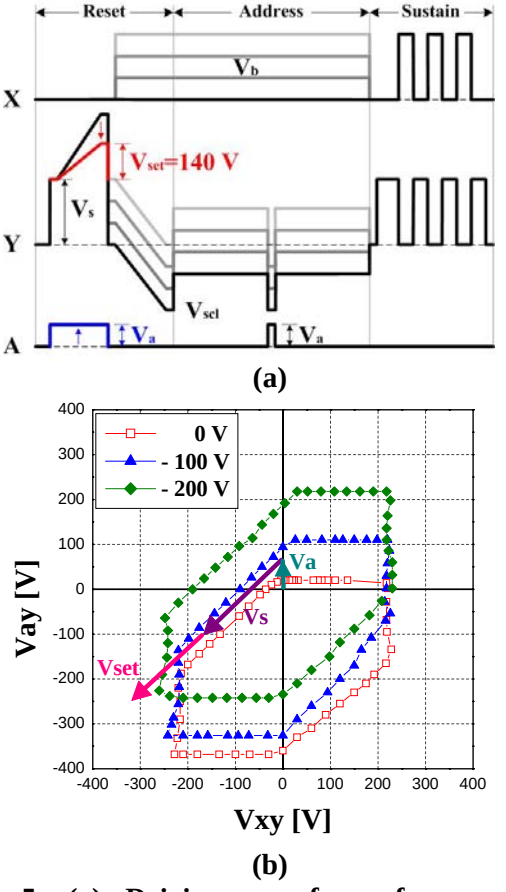

Fig. 5. (a) Driving waveform for preventing unstable reset discharge and (b) proposed reset voltage vectors on V_t close-curve on applied voltage plane.

100 V, the ions are accumulated on the X and Y electrodes, whereas the electrons are accumulated on the A electrode, as shown in Fig. 4 (b). However, for the lower scan-low voltage case (-200 V), the wall charges formed by the reset discharge in a cell are eliminated and begin to be accumulated with opposite polarity between the Y and A electrodes compared with the conventional case. That means, in the conventional case after a reset period, the electrons are accumulated on the X and Y electrodes and the ions are accumulated on the A electrode, however, in this case, the electrons are accumulated on the A electrode. As shown in Figs. 2 and 4 (b), it is found that the address discharge time lags of the lower scan-low voltage cases (-150 and -200 V) are shortened when the wall charges are eliminated in a cell and applied voltage is increased compared with the case of having a large amount of wall charges.

In the case of the conventional reset procedure, the applied voltage vectors, as shown in Fig. 4 (b), is moved to diagonal direction and the discharge firing is produced on the fourth side of the V_t close-curve. Therefore, the stable reset discharge is produced between the Y and X electrodes in the fourth side, because of the discharge between the MgO surfaces. However, the unstable reset discharge is shown in Fig 3, which is caused by the phosphor cathode condition when applying the rising-ramp waveform because the applied voltage vector is moved to the fifth side, as shown in the V_t close-curve of Fig. 3 [5]. During the falling-ramp period, the stable discharge is obtained easily because the voltage vector is moved to the first side with an MgO cathode condition. That is, the reset discharge is mainly produced between the Y and A electrodes because the wall charges are accumulated oppositely on three electrodes by the changes of the voltage between the Y and A electrodes at the constant voltage between the X and Y electrodes.

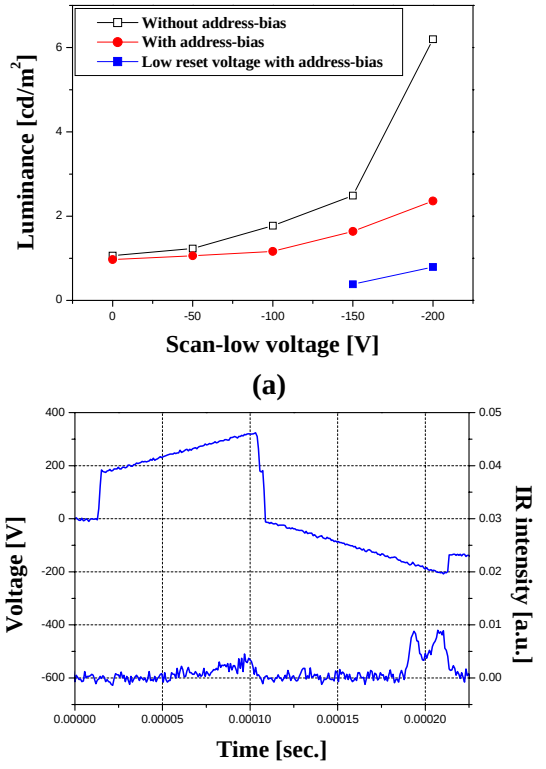

Fig. 6. (a) Changes in background luminance with decrease in scan-low voltage and (b) IR emission waveforms during reset period when applying proposed driving methods.

4. Proposed Driving Methods

For preventing the unstable reset discharge by production of a plate-gap discharge between the Y and A electrodes during a reset period, the address-bias voltage is applied during a rising-ramp period in a reset period with the same voltage level during an address period, as shown in Fig. 5 (a). This address-bias voltage can block the plate-gap discharge between the Y and A electrodes during a reset period, and induce the surface discharge between the X and Y electrodes for the stable discharge. By the address-bias voltage, the voltage vector during a rising-ramp period is moved to the fourth side and the stable reset discharge is found in Fig. 5 (b). By the way, though the address-bias voltage can prevent the unstable reset discharge, the background luminance is still high. To reduce the background luminance, the reset voltage is decreased under the same address discharge characteristics as shown in Fig. 5 (a).

Fig. 6 (a) shows the changes in the background luminance with a decrease in the scan-low voltage in the case of without/with an address-bias voltage applied to the address electrode during a rising-ramp period in a reset period, and low reset voltage with an address-bias voltage. Without an address-bias voltage, the background luminance is increased significantly with a decrease in the scan-low voltage. When applying the address-bias voltage, the background luminance is decreased, especially in the case of a low scan-low voltage. As a result of adopting the low reset voltage with an address-bias voltage, it is found that the background luminance is considerably reduced and the stable reset discharge is produced without delaying an address discharge time, as shown in Fig. 6 (b). From 0 to -100 V of the scan-low voltages, the address discharge is fail and weakly produced compared with the low scan-low voltages.

5. Conclusion

This work focuses on investigating the amount of wall charges by the various applied voltages based on the IR emission and V_t close-curve analysis. It is found that the improved address discharge characteristic is caused by the effect of the higher external applied voltage during an address period than the accumulated wall charges during a reset period. The background luminance can be reduced in the case of the low scan-low voltage by applying the address-bias voltage during a rising-ramp period for preventing the plate-gap discharge during a reset period between the Y and A electrodes and by decreasing the reset voltage.

5. References

1. S. Kanagu, Y. Kanazawa, T. Shinoda, K. Yoshikawa, and T. Nanto, *SID'92 Technical Digest*, p713 (1992).
2. M. Amatsuchi, A. Hirota, H. Lin, T. Naoi, E. Otani, H. Taniguchi, K. Amemiya, *SID'05 Technical Digest*, Vol. **1**, p435 (2005).
3. J. S. Kim, J. H. Yang, T. J. Kim, and K. W. Whang, *IEEE Trans. Plasma Sci.*, p1083 (2003)
4. H. J. Kim, J. H. Jeong, K. D. Kang, J. H. Seo, I. H. Son, K. W. Whang, C. B. Park, *SID'01 Technical Digest*, p1026 (2001)
5. K. –H. Park, S. –K. Jang, H. –S. Tae, J. –H. Seo, and S. –H. Lee, *IDW'05 Technical Digest*, p1445 (2005)