

A novel integrated a-Si:H gate driver

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Abstract

A novel integrated a-Si:H gate driver with high reliability has been designed and simulated. Since the a-Si:H TFT is easily degraded by gate bias stress, we should optimize the circuit considering the threshold voltage shift. The conventional circuit shows voltage drop at the input stage by threshold voltage of the TFT, however, the proposed circuit dose not shows voltage drop and keeps constant regardless of threshold voltage shift of the TFT.

1. Introduction

Amorphous-silicon thin-film transistors (TFTs) are well known as switches associated with pixel elements in active matrix liquid-crystal displays (AMLCDs). Their key characteristics are a rather low field effect mobility (0.5 cm²/V-sec), a low leakage current in the OFF state (< 0.1 pA for V_{ds} = 10 V at V_{gs} = -5 V), and uniform TFT parameters over very large surfaces. In spite of low field effect mobility these TFTs can also be used to build the row drivers of the AMLCD directly on glass with simple circuit schematics [1],[2].

Integrating of drive circuits in TFT backplane is of increasing interest because of many advantages such as overall cost reduction, compactness and mechanical reliability. Because of the high mobility (50~300cm²/V-s), Poly-Si TFT is suitable for driver integration, it can be used in system on glass (SOG), where the memory, sensor, microprocessor and control circuits are integrated in addition to drivers. However, the manufacturing cost of poly-Si TFT backplane is much higher than that of a-Si:H. On the other hand, the integrated circuit using a-Si:H TFT has several advantages. First, most of the TFT-LCD

manufacturers are based on a-Si:H TFT technology. Second, a-Si:H TFT process is suitable for large area applications because of its low cost, low temperature processing and better uniformity over large area substrates. Third, the module cost can be reduced by eliminating the drive IC's and related processes.

However the main problem encountered when running them is the shift of the threshold voltage (V_T) of the TFT under operation, which is induced by charge trapping into the insulator and the increase of the number of defects in the a-Si:H channel [3],[4],[5]. These properties are not avoidable and induce instability of the gate driver during operation. This leads to a drop of the ON current of the TFT that prevent normal operation of the drivers. Figure 1(a) shows the conventional a-Si:H circuit suggested by Thomson to overcome the low mobility a-Si:H TFT and until now many applications have been suggested to improve the reliability of the circuit [6],[7],[8].

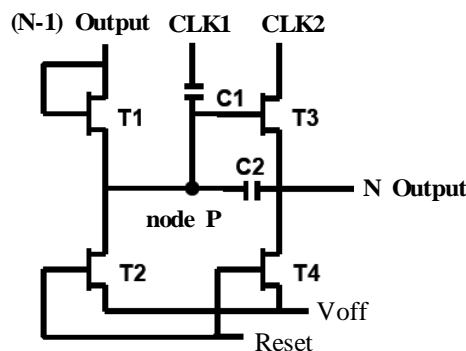


Figure 1. (a) The conventional scheme

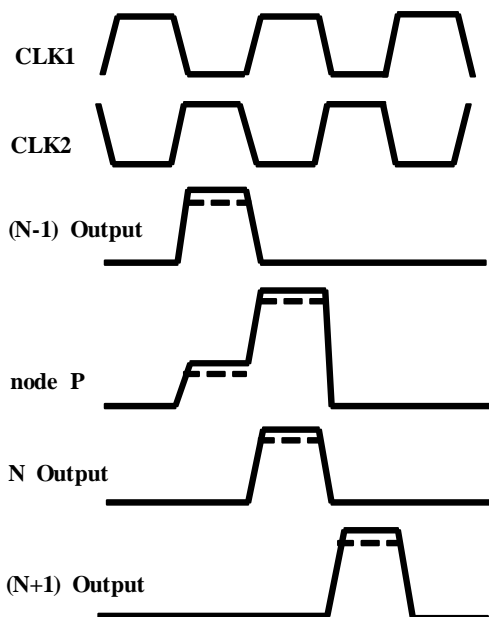


Figure 1. (b) timing diagram of gate driver.

2. Experimental

In this paper, we propose a new gate driver with high stability as shown in Figure 2. Figure 1 (a) is the conventional schematic. Figure 1 (a) shows one stage of the shift register of conventional a-Si:H TFT gate driver. The output of the previous stage is supplied to the input. The reset is supplied by the next stage output. The previous output applies to the P node through the T1 transistor. The P node voltage is less than input voltage by the threshold voltage of T1. The proposed new scheme has no voltage drop at the P node. Therefore this can improve reliability of a-Si:H gate driver. Although threshold voltage of T1 TFT increases, the voltage of the P node is not changed. Figure 1(b) is the timing diagrams of the a-Si:H TFT gate driver. The output of the previous stage is (N-1) output, and the next stage output is represented by (N+1) output. The voltage at the node P is increased when (N-1) output goes high and much more increases when N output goes high by the capacitive coupling between output node and the P node. The N output reset to the Voff when (N+1) output goes high. The dotted line is for the conventional circuit and the full line is for the proposed one.

In this work the channel widths and lengths of TFTs were from $W/L = 3,000/4\mu\text{m}$ to $W/L = 7,000/4\mu\text{m}$, and the capacitance of capacitors was 5pF.

We also considered parasitic capacitance (C_{gs} , C_{gd}) [9]. To achieve enough drive ability of the circuit output, the channel W/L of TFTs should be high. The bigger the channel W/L of TFTs, the higher voltage fluctuation results in by parasitic capacitance. So we have properly designed to achieve a better output and the less effect of parasitic capacitance.

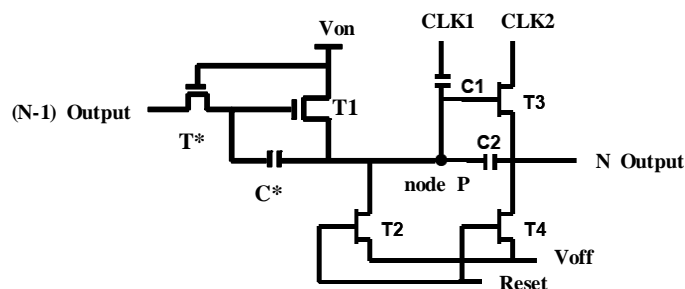


Figure 2. The proposed circuit is reconstructed by T*, C* which can keep input high level without decrease.

3. Results and discussion

The proposed circuit is shown in Figure 2. The new circuit prevents the voltage drop at the P node, therefore it provides long life time circuit because the P node voltage is the gate voltage of transistor T3. To achieve this no loss of input voltage we used one more transistor T* and a coupling capacitor C*.

Figure 3(a) shows the simulation results for the conventional and the proposed circuit. The voltages at the node P and the output voltages are shown at Figure 3(a). The simulation shows higher voltage of the P node for the proposed circuit than conventional one.

When the threshold voltages of T1 and T* increase, the P node voltage decreases for the conventional circuit, however does not decrease for the proposed one. Therefore, the life time of the proposed circuit is longer than the conventional one.

Figure 3(b) shows that the shorter channel width is allowed for the proposed circuit since the P node voltage is higher than the conventional one. Small channel width can minimize unnecessary effect that happen by parasitic capacitance of TFT. The parasitic capacitance induces fluctuation of output, which is applied to the input of the next stage. Therefore, the fluctuation of the output voltage results in unstable operation of the gate driver. The stability of the circuit is improved by reducing the parasitic capacitance.

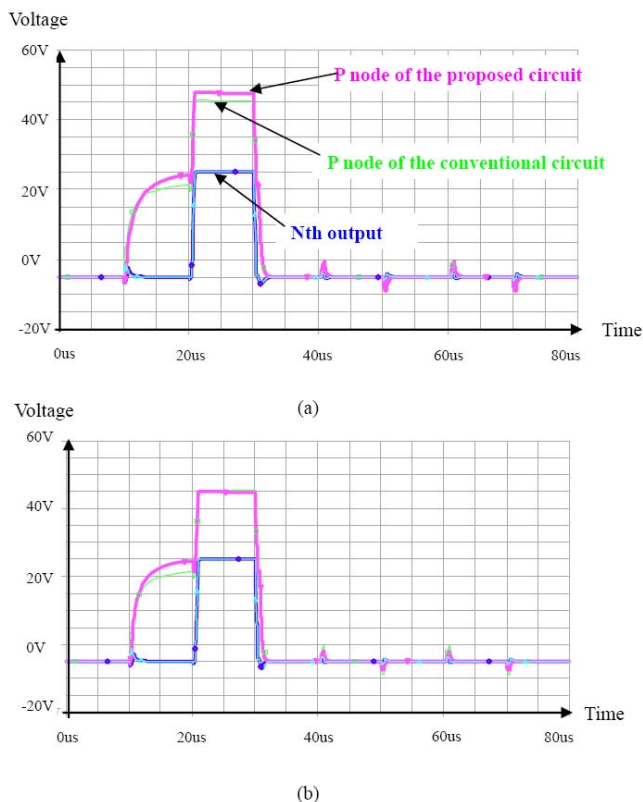


Figure 3. The simulation results of new a-Si:H gate driver and the conventional gate driver. (a) Output of the proposed circuit and the conventional one at the equal channel width of T3 TFT, (b) at the proposed circuit we can get output same as the conventional circuit even if reducing T3 TFT width

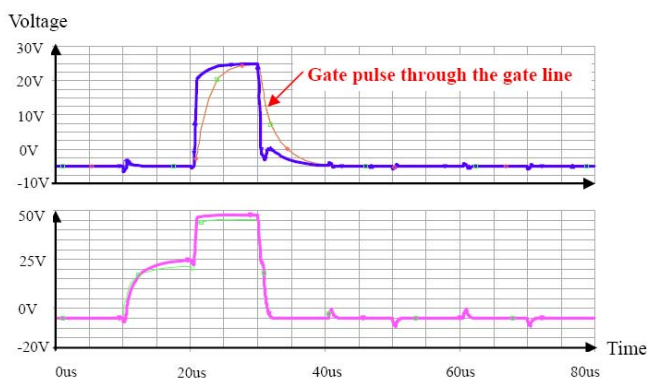


Figure 4. Gate output on the panel gate line

The proposed circuit is on the process. After fabrication of the circuit the life time of the gate driver will be compared between the conventional one and the proposed one.

4. Summary

We have achieved good stability from the proposed gate driver with a-Si:H TFT. To apply this circuit to the large size TFT LCD (TV, Monitor), we should minimize the influence of TFT's parasitic capacitance. Therefore, the proposed circuit is suitable for large size TFT LCD as well as mobile display. Figure 4 shows that gate pulse on the gate load is good enough for the operation of large size TFT LCDs.

5. References

- [1] H. Lebrun, N. Szydlo, F. Maurice, T. Borel, R. G. Stewart, S. Weisbrod, and R. Huq, SID 96 DIGEST, 677, 1996.
- [2] H. Lebrun, F. Maurice, J. Magarino, N. Szydlo, SID'95 DIGEST, 403, 1995.
- [3] H. Lebrun, Nicolas Szydlo, Eric Bidal, Journal of SID 11/3, 539, 2003.
- [4] M.J. Powell, Appl. Phys. Lett 43(6), 597, 1983.
- [5] M.J. Powell, Appl. Phys. Lett 60(2), 207, 1992.
- [6] Jae Hwan Oh, Ji Ho Hur, Young Duck Son, Kyu Man Kim, Se Hwan Kim, Eun Hyun Kim, Jae Won Choi, Sung Man Hong, Jin O Kim, Byung Seong Bae, and Jin Jang, SID'05 Digest 943, 2005.
- [7] Ja Hun Koo*, Jae Won Choi, Young Seoung Kim, Moon Hyo Kang, and Jin Jang, IMID/IDMC '06 DIGEST 1271, 2006.
- [8] Jin Jeon, Kyo-seop Choo, Won-Kyu Lee, Jun-ho Song, Hyung-guel Kim, SID 04 DIGEST, 11, 2004.
- [9] M.J. Powell, IEEE Vol. 36, No. 12, 2753, 1989.