Stress Estimation of a Drain Current in Sub-threshold regime of amorphous Si:H

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Abstract

We have investigated the threshold voltage shifts (ΔVth) and drain current level shift (ΔIds) in sub-threshold region of a-Si:H TFTs induced by DC Bias (Vgs and Vds) - Temperature stress (BTS) condition. We plotted the transfer curves and the ΔVth contour maps as Vds-Vds stress bias and Temperature to examine the severe damage cases on TFTs. Also, by drawing out the time-dependent transfer curve (Ids-Vgs) in the region of $10^{-8} \sim 10^{-13}$ (A) current level, we can estimate the failure time of TFTs in a operating condition.

1. Introduction

In the LCD and AMOLED display based on a-Si:H TFT, there have been a lot of concerns for the reliability of image quality and life time of display. As increasing the using time, the electrical properties of display is degraded because of electrical instability of a-Si:H TFT. This electrical instability has explained with two mechanisms [1-4]. One is the charge trapping in the gate insulator, which makes the transfer characteristics parallel shifted. And the other mechanism is state defect creation at/ or near the a-Si:H / gate insulator interface, which makes the sub-threshold slope (S-factor) increase and degenerates the switching ability of TFTs. The instability of TFTs in BTS is mixed with above two mechanisms and depends on the manufacturing process and environment [5].

This electrical instability of TFTs caused a lot of reliability issues on the image quality. Though initial LCD products have no fault, after several years they starts to be revealed the faults such as mura, vertical cross-talk, etc. Especially, the vertical cross-talk is one of the most frequently revealed faulty, which are caused by off-state Ids current level in sub-threshold region. Therefore, in this paper, we focused the ΔIds

current level as well as ΔVth shift varied with stress time.

2. Experimental

We have examined the electrical instability with the inverted staggered bottom-gate a-Si:H TFTs. We used the individual TFT for a BTS condition. All TFTs in this paper have about 4000 Å thick a-SiNx:H as a gate insulator layer, 2000 Å thick a-Si:H as a active layer and 500 Å thick n$^+$ layer between Drain/Source electrode and a-Si:H layer. Also, TFT size, W/L is = 24 / 5 um. And these TFTs were manufactured by the same design and process. Measurement procedures are (1) measuring the pre-stressed transfer characteristic, (2) applying stress as a function of stress time in the given BTS condition and (3) measuring post-stressed transfer characteristic, afterward repeating (2) and (3) for the time-dependent BTS condition. The HP4156C semiconductor Analyzer is used for the measurement and bias stress.

3. Results and discussion

In the light of LCD operation, the TFT is always stressed by varing Vgs and Vds during holding time region. Because all Vgs and Vds bias condition affects to the TFT instability [9], we first examined the ΔVth shift as functions of the stress Vgs and Vds bias at the constant stress time (1000sec). Figure 1 and 2 show the transfer characteristics and contour plots of ΔVth, respectively. In figure 2, Vth was mainly shifted by Vgs stress not Vds, because the contour lines vary along the Vgs bias axis (x-axis). It indicates that main cause electrical instability of the TFT is the Vgs bias. So, we have focused the stress Vgs bias and among the rest, the negative bias. Because all gate biases remain in the negative bias during the holding time

region. Moreover the holding time region is much longer than the charging time region (Vgs is positive). For example, in case of the UXGA LCD panel, the ratio holding time and charging time is 16654us / 12.5us (1332 times).
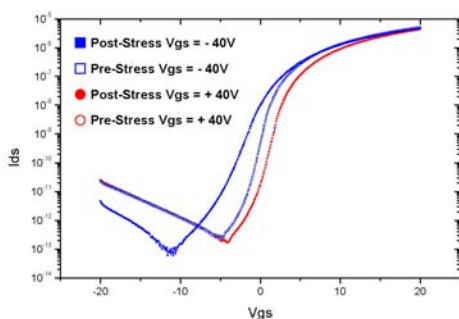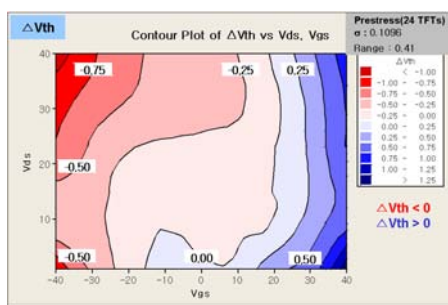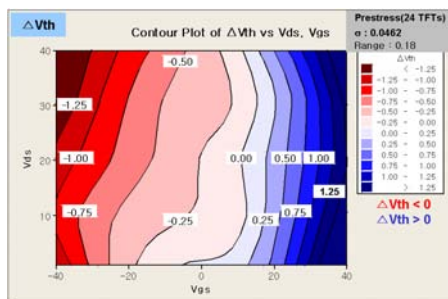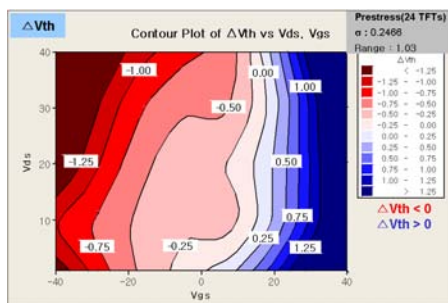

Figure 1. The pre-stressed (open symbols) and post-stressed (solid symbols) transfer curves. BTS conditions are stress Vds = 10V, stress time = 1000 sec and temperature = 60℃.

a) Room Temperature

b) 60℃

c) 80℃

Figure 2. The contour plots of △Vth as a function of stress Vgs and Vds in (a) Room Temperature, (b) 60℃ and (c) 80℃. Stress time is fixed in 1000 sec. Their standard deviations and ranges on the Vth of pre-stressed TFT are demonstrated in the plot boxes.

Also, figure 1 shows the pre-stressed and post-stressed transfer curves (measurement Vds = 15V) of TFTs. In the positive Vgs stress condition, the transfer curve shifted the parallel positive direction and in the negative, transfer characteristics shifted the negative direction and degraded the sub-threshold slope (S-factor). In respect of leakage current during holding time region, the negative Vgs is more severe stress than the positive.

For estimation on the reliability of display quality, we have monitored the ΔVth as a function of stress time. Also, we have defined the V_{min} as the voltage at the minimum Ids in electron conduction region to estimate the Ids level in sub-threshold regime. Figure 3 (a) shows ΔVth and (b) ΔV_{min} as a function of stress time. About ΔVth, previous reports [1, 6-8] well described it as the form of a stretched exponential function.

$$\Delta Vth(t_{stress}) = \Delta Vth_O \cdot \left\{ 1 - \exp\left[-\left(\frac{t_{stress}}{\tau} \right)^{\beta} \right] \right\} \qquad (1)$$

With

$$\Delta Vth_O = \Delta Vth(\infty) = Vgs^{stress} - Vth(0) \qquad (2)$$

where ΔVth_O is the shift at infinite time, τ is a characteristics time constant, and β is the stretched-exponential exponent which is temperature-dependent.

For the ΔV_{min} Fitting, we have drawn out the simple equation from a relationship of ΔVth and $\Delta V_{min,}$ as following,

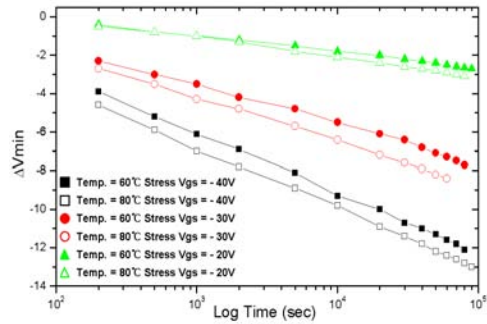$$\Delta V_{min} = A(stress\_Vgs) \cdot \Delta Vth^{\beta'(stress\_Vgs)} \qquad (3)$$

where A and β' are fitting parameters which depends on the stress Vgs bias. the figure 4 shows measurement values and the fitted curve obtained by eq. (3)

Finally, It is important to estimate the Ids level in the region of sub-threshold. So, we also have fitted the Ids shifted by the stress [10]. As functions of,

$$\Delta Ids = f \,(Stress\, Vgs,\, Temperature,\, Stress\, time, \\ Measurment\, Vgs)$$
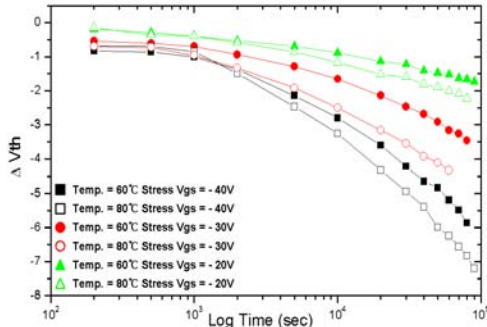
a) The stress time dependency of $\triangle$Vth

b) The stress time dependency $\triangle$Vmin

Figure 3. (a) The $\triangle$Vth and (b) $\triangle$Vmin as a function of stress time in 60℃ (solid symbols) and 80℃ (open symbols) BTS condition. The square($\square$) symbols stands for the stress Vgs = -40V, circles($\bigcirc$) -30V and triangles($\triangle$) -20V, respectively.
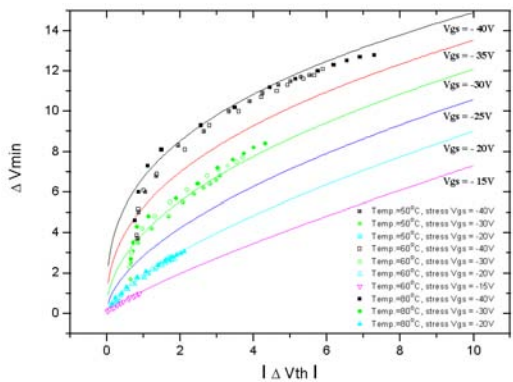

Figure 4. This graph shows the relationships of $\triangle$Vth and $\triangle$Vmin. The calculated curves (lines) and the measurement values (symbols) of $\triangle$Vmin as a function of $\triangle$Vth absolute value. The fitting curves are calculated from eq. (3).

That is,

$$\Delta Ids = A_{Temp} \cdot (\Delta Vth(t))^{\beta_{Temp}} \times A_{Vgs} \cdot (\Delta Vth(t))^{\beta_{Vgs}}$$

So,

$$\Delta Ids = A(Temp, Stress\_Vgs) \times (\Delta Vth)^{\beta(Temp, Stess\_Vgs)} \quad (4)$$

Where,

$$A(Temp, Stess\_Vgs) = A_{Temp} \times A_{Stress\_Vgs}$$
$$\beta(Temp, Stress\_Vgs) = \beta_{Temp} + \beta_{Stress\_Vgs}$$

also, from equation 1 and 2, we can plot the ΔVth as the following form,

$$\Delta Vth(t) = A \cdot t^{\beta} \quad (5)$$

Finally, we can estimate the Ids at any stress time by mixture of the equation (4) and (5).

Figure 5 shows the fitted (dotted lines) and measured (solid lines) Ids-Vgs curves at the given stress time and BTS condition. From this curve fitting, we can estimate the Ids level at any using time, any operation voltage, and any operation temperature.
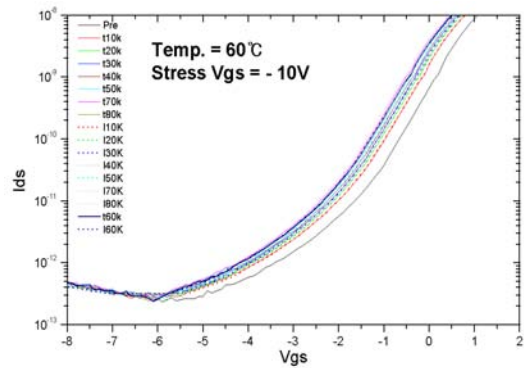
a) stress Vgs = -10V and 60℃
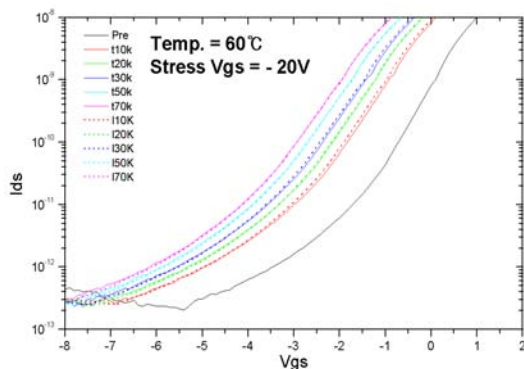
b) stress Vgs = -20V and 60℃
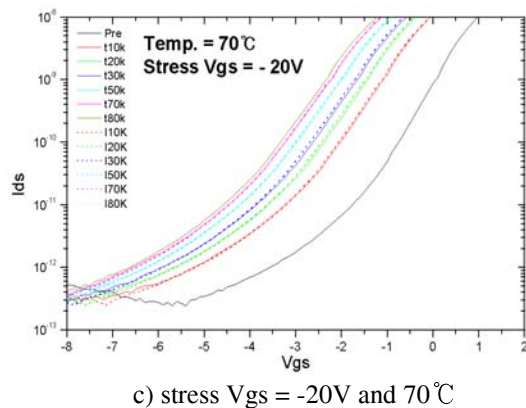
c) stress Vgs = -20V and 70℃

Figure 5. The transfer curves of pre- and post- stressed TFTs with various stress time. The solid lines indicate the mearsured curves and dotted lines fitted curves with eq (4). Stress time and stress conditions are demonstrated in the plot boxes.

4. Summary

As increasing LCD demands, image quality of worn-out LCD panel as well as the initial LCD is getting important. So a lot of the reliability tests have been done in the LCD industry. However, almost reliability tests are based on the LCD module and need to high cost and long time. Therefore, we have tried to change module based tests to the TFT. Among the faults in reliability tests, especially vertical cross-talk is one of the most frequently revealed faulty in reliability test. Such vertical cross-talk is described that the stress degenerates the transfer characteristics of TFT and shifts up the leakage current level in holding time region after any stress time. So we have investigated electrical instability of TFT in terms of ΔIds as well as ΔVth. From the ΔIds fitting curve, we can estimate the leakage current level under operation. It enables us to expect time on the failure caused by the leakage current and to replace the large amount module based reliability test by the TFT based.

5. References

1. W. B. Jackson and M. D. Moyer, Phys. Rev. B **36**, 6217 (1987)
2. M. J. Powell, C. van Berkel, and A.R. Franklin, Phys. Rev. B **45**, 4160 (1992)
3. M. J. Powell and S. C. Deane, Phys. Rev. B **48**, 815 (1993)
4. Y. Tai, J. Tsai, and H. Cheng, Appl. Phys. Lett. **67**, 76 (1995)
5. J. Tsai, C. Huang, Y-H. Tai, H-C. Cheng, F-C. Su, F-C. Luo, and H-C. Tuan, Appl. Phys. Lett. **71**, 1237 (1997)
6. S. Jahinuzzaman, A. Sultana, K. Sakariya, P. Servati, and A. Nathan, Appl. Phys. Lett. **87**, 023502 (2005)
7. C. Chiang, J. Kanicki, and K. Takechi, Jpn. J. Appl. Phys. **37**, 4704 (1998)
8. M. J. Powell, C. van Berkel, and J. R. Hughes, Appl. Phys. Lett. **54**, 1323 (1989)
9. K. Karim, A. Nathan, M. Hack, and W. Milne, IEEE. Electron Dev. **25**, 188 (2004)
10. S. Jahinuzzaman, P. Servati, and A. Nathan, Proc. of SPIE. **5578**, 3151. G. W. Scherer, *J. Am. Ceram. Soc.,* **73[11]**, 3 (1990).