a-Si TFT based systems on TFT-LCD panels

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Abstract

Integrating systems on TFT-LCD panels is more and more popular for the mobile display application. However, it may not be necessary to use LTPS TFT devices. A-Si TFTs are used to integrate systems on TFT-LCD panels, especially scan (gate) drivers. To further reduce the chip size of driver IC, the triple-gate pixel structure is developed. Therefore, the number of the source lines is reduced to 1/3 times.

1. Introduction

In resent years, the market demand of mobile applications for high resolution displays has been increased dramatically. Accordingly, TFT-LCD panels with high resolution specifications have been widely used. Generally, the cost of driver ICs would increase with the resolution of displays. Therefore, driver systems integrating on panels by TFTs have been proposed many years to meet the requirement on cost reduction. For ten years, people used LTPS TFT devices to fulfill the concept of system on panels. However, in some way, because that the yield rate of a-Si TFT-LCD generally is higher than LTPS TFT, the approach to use a-Si TFT has not been given up.

It has been already demonstrated that a a-Si TFT-LCD panel with high pixel density (2.2” QVGA & 2.47” VGA) can be achieved by integrating gate driver circuit on glass [1, 2]. As a result, there is no need of gate driver IC. However, it still needs source driver IC, and the number of source lines is 720 for QVGA and 1440 for VGA. If we’d like to further reduce the chip size of the source driver IC, it is suggested to integrate demultiplxer switch on the a-Si TFT panels like using demultiplexer on LTPS TFT-LCD panels. However, in this paper, we didn’t choose this approach.

In this paper, we discussed a different pixel scheme, which could reduce the number of source lines but increase the number of gate lines. Fig. 1 shows this different triple-gate pixel structure compared to the normal pixel structure. For normal pixels, each pixel is composed of three stripe arranged RGB subpixels and controlled by one gate line and three data lines. On the contrary, in the triple-gate pixel structure, the RGB subpixels are rotated in the layout and controlled by three gate lines and one data line for display. Hence, the number of data lines reduces to 1/3 times as many as the normal pixel structure, but the number of gate lines increases by 3 times. In order to realize what mentioned above, we could use the design of RASD (reliable a-Si scan driver) as alternative integrated on glass to substitute conventional gate driver IC; therefore, the chip size of source driver IC (signal chip driver IC) would be reduced, as shown in Fig. 1.

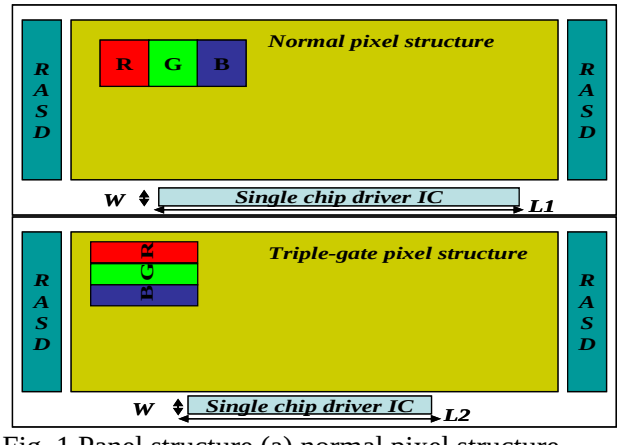

Fig. 1 Panel structure (a) normal pixel structure (b) triple-gate pixel structure

It has been well known that a-Si TFT has characteristic of not only poor mobility but also stress issues. Although there is still difficulty to use a-Si TFT based systems on panel, we succeed to create reliable scan driver circuits in which integrate a-Si TFT devices with longer lifetime on both of our QVGA (320 gate lines) and VGA (640 gate lines) normal pixel structure panels. In this paper, we propose a new RASD circuit design and evaluate the feasibility. More specifically, we converted the normal pixel structure with prior RASD circuit into a triple-gate pixel structure with the new RASD circuit. For QVGA resolution, the triple-gate pixel structure with the new RASD circuit needs 960 gate stages.

2. Prior RASD circuit

The schematic diagram of a prior RASD circuit shown in Fig. 2 illustrates that the RASD operates with 2-phase clock signals and a start pulse, which are either Vdd (high level) or Vss (low level). Each of the circuit 1 and circuit 2 can prevent node P2 and output signal Vout(i) from being in a floating state. Meanwhile, the RASD including circuit 1 and circuit 2 still can function well even when the threshold voltage of a-Si TFT in circuit 1 and circuit 2 increases to a specific level (2/3(Vdd-Vss)).

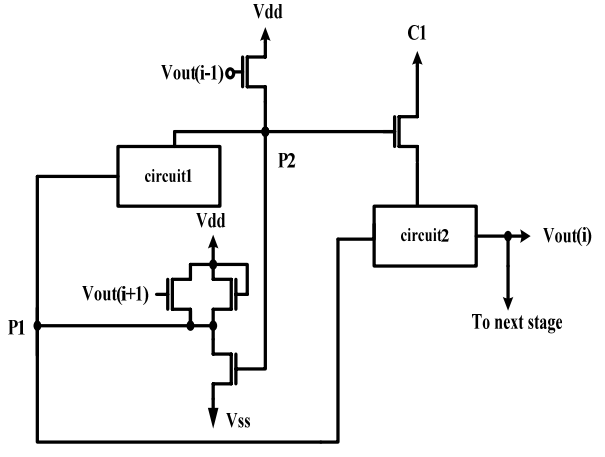

Fig. 2 The schematic diagram of prior RASD circuit for 2.2" QVGA and 2.47″ VGA panels

According to the result of software simulation, the RASD operates normally until Vth of a-Si TFT, which is provided by a sustained voltage stress for a long time, increases to 2/3(Vdd-Vss). According to the characteristic curves of an a-Si TFT device derived from the stress experiment, it could be predicted that the Vth of a-Si TFT would increase to 2/3(Vdd-Vss) after at least 50,000 hrs. In conclusion, the lifetime of the RASD is expected to be over 50,000 hrs based on the experiment mentioned above.

3. New RASD

For QVGA triple-gate pixel structure, the number of gate stages is 960. That means we need more current driving capability for the RASD circuit. So we propose a new RASD circuit to meet the requirement. The schematic diagram of the new RASD as shown in Fig. 3 illustrates that the RASD operates with 3-phase clock signals and a start pulse, which are either Vdd (high level) or Vss (low level). Furthermore, circuit 1 and circuit 2 are operated by the control signals from the $(n+2)^{th}$ shift register stages. In other words, the operation of the n^{th} shift register unit of the new RASD circuit is not controlled by the output signal of the n^{th} or $(n+1)^{th}$ shift register unit. Consequently, the new RASD circuit demonstrates shorter delay time of the output signal, and the LCD applying this new RASD circuit of this implementation further has the advantage of the better quality of the display performance.

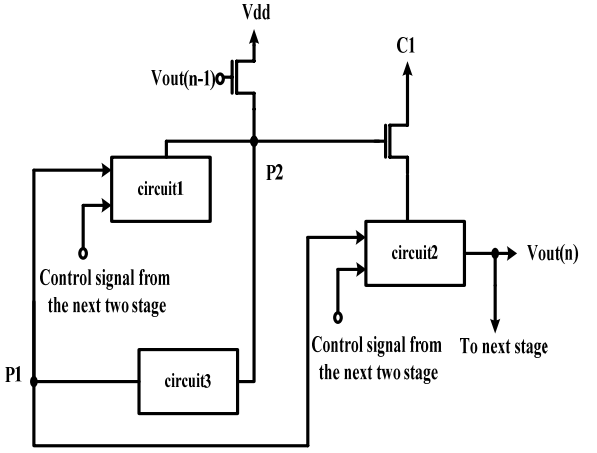

Fig. 3 The schematic diagram of new RASD for the 2.69″ QVGA panel

In addition, the new RASD circuit in the Fig. 3 consists of circuit 3 units for preventing the circuit from abnormal operation under low temperature. The prior RASD circuit (Fig. 2) is influenced by the stress effect and gradually operates abnormally in the long run operation under the low temperature. On the contrary, the new RASD circuit prevents the leak current through the NMOS inverter circuit and performs be insensitive to the temperature.

4. TFT device

In addition to the new RASD circuit design, it is also improved the I-V characteristics of a-Si TFT device for the triple-gate pixel structure panels. The improving performance is shown in Fig. 4, which compares new TFT device with old TFT device. To evaluate the performance of the new RASD with new TFT device, we fitted the new TFT device model and run SPICE simulation for the new RASD circuit. Consequently, we found a very different result at low temperature environment. The prior RASD circuit applied in the normal pixel structure operated well at the low temperature. But some problems occurred in the triple-gate pixel structure by use of the prior RASD at the low temperature. However, the new RASD design applied in the triple-gate pixel structure shows better driving performance and operate well under the low temperature environment (-30℃) ,as shown in Fig. 5.

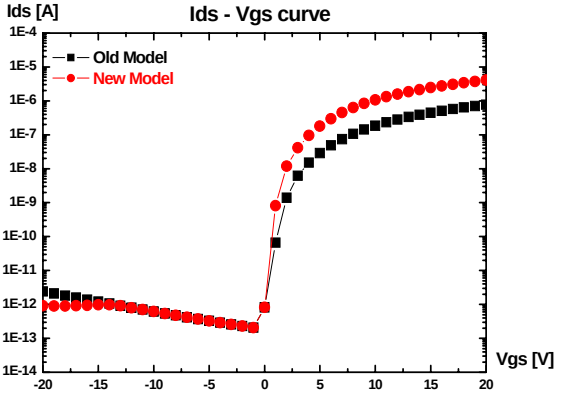

Fig. 4 Comparison of a-Si TFT I-V characteristics with the new and the old devices.

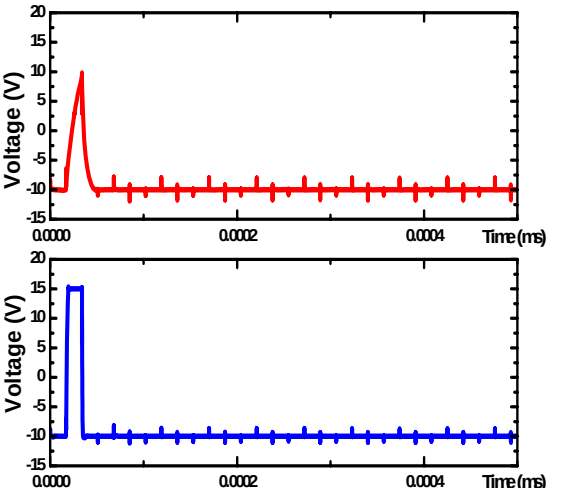

Fig. 5 Comparison of a gate output pulse waveform simulated with the new RASD and the prior RASD at the low temperature (-30℃).

5. Architecture

The double-sided RASD driving scheme is applied in the panel layout, as shown in Fig. 6 Fig. 7 shows the time-domain signals. The double RASD consists of 4 input signals. STP, CK1, CK2 and CK3 are input signals that are applied to odd part of the double-sided RASD. Also, STP, CK1, CK2 and CK3 are input signals that are applied to even part of the double-sided RASD. The operational principle of each part of the RASD circuits is the same as that of the single-sided RASD.

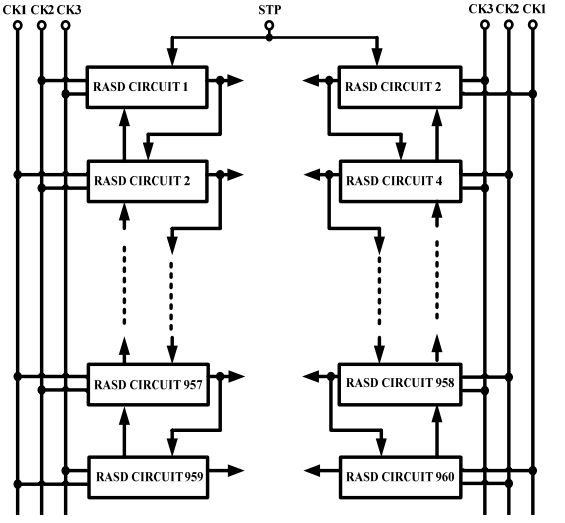

Fig. 6 Block diagram of double-sided RASD circuit

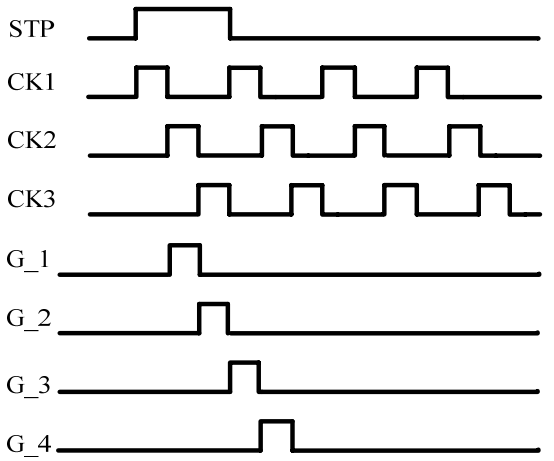

Fig. 7 Time-domain signals of double-sided driving

6. Display performance

Fig. 8 shows the display image of 2.69” QVGA triple gate panel. Table1 shows the specification of 2.69” QVGA panel.

Table1 Panel specification

Diagonal Size	2.69 inch
Resolution	240x320xRGB
Display Color	262K colors
Contrast Ratio	>500:1
Luminance	200cd/m2
NTSC Ratio	50%

Fig. 8 Display image of 2.69” QVGA panel

7. Conclusion

We developed a double-sided RASD with triple-gate pixel structure technology to get the benefit of saving a gate driver IC, reducing the chip size of a driver IC, and the cost saving as a whole. In addition, we selected a-Si TFT-LCD panels instead of LTPS TFT-LCD panels to integrate the new RASD on the glasses and the result is fully satisfied. It means even though we don’t use LTPS technology to integrate scan driver circuits on a glass, we still acquire an acceptable performance by normal a-Si technology.

8. References

[1] His-Rong Han Ja-Fu Tsai, Wen-Tui Liao, and Wen-Chun Wang, SID Technical Digest, pp946-949(2005).

[2] His-Rong Han Ja-Fu Tsai, Wen-Tui Liao, and Wen-Chun Wang, IDW, 2005.