High Efficiency and Small Area DC-DC Converter for Gate Driver using LTPS TFTs

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Abstract

A new DC-DC converter was designed for gate driver circuit using low temperature poly-Si TFT technology. To achieve high efficiency and small area, we proposed a cross-coupled type DC-DC converter which converts 5V of input voltage to 9V of output voltage and supplies 120μA of current to load. Its efficiency is 92.9% and the area is reduced as much as 19% compared to the previously reported latch type DC-DC converter.

1. Introduction

Mobile applications such as cellular phone, PMP (portable multimedia player) and digital camera require display systems with compact size, high quality image, low power consumption and low cost. LTPS (Low Temperature Polycrystalline Silicon) technology has a great potential to integrate the driver circuits and the power management circuits with pixel array on a glass substrate [1]. Therefore, compact size and low cost display system can be achieved using LTPS technology because the driver circuits, which are integrated on glass substrate, substitute driver ICs.

But, because all of the peripheral circuitries cannot be integrated altogether, the display system based on LTPS technology still needs a lot of external devices. These external ICs prevent lowering the cost of the display system because they take up a large portion of overall system cost. As a result, it is very desirable to increase the integration level of poly-Si circuit to reduce the overall module cost.

Furthermore, in the case of integrated gate driver in LTPS TFT panel, because the TFTs need very wide voltage range around 20V, additional supply voltage levels are needed in addition to the logic supply voltages. The ICs to supply or using those of high voltages, like DC-DC converters or voltage level shifters, are expensive because they require high-voltage-handling process. To increase the cost-competitiveness of display system using LTPS TFTs, integrating highly efficient DC-DC converter on the glass substrate using LTPS TFT circuit technology is indispensable[2].

2. The previously reported DC-DC converter

Figure 1(a) shows the schematic diagram of previously reported latch type DC-DC converter. This structure supplies power to the load in high speed by charging the output capacitor both in ‘high’ and ‘low’ state of the clock signals. But, in this type of DC-DC converter, on-resistance of the driving TFTs is relatively high because the gate voltage range of

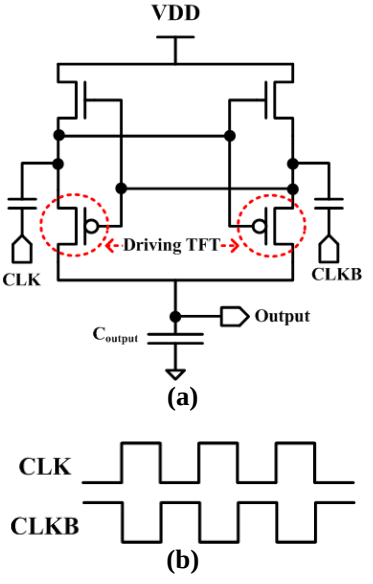

Fig. 1. The previously reported latch type DC-DC converter : (a) Schematic diagram and (b) waveforms of input clock signals.

driving TFTs is the amount of VDD, i.e. between VDD to 2VDD not GND to 2VDD. The large on-resistance makes the width of the driving TFTs and the coupling capacitor size large. This also leads the clocking power to be increased.

Thus we proposed a new cross-coupled type DC-DC converter which decreases the on-resistance of the driving TFTs by making the gate voltage of driving TFTs have range from 0 to 2VDD.

3. The proposed DC-DC converter

Figure 2(a) shows the schematic of the proposed DC-DC converter. The initial voltage at node1 is set to VDD. As shown in the figure 2(a), the voltage at node1 rises to 2VDD when the CLK signal becomes 'High' and the CLKB signal becomes 'Low'. The voltage at node1, 2VDD, turns on the N2 TFT and the node2 is charged to VDD. Correspondingly, the voltage at node2 turns on the P4 TFT and the voltage at node1 transferred through P1 and P4 TFT to P2 TFT and the P2 TFT is turned on. At the same time, P1 TFT is turned on by setting the gate voltage of the P1 TFT to 0V. It means driving TFTs have lower turn-on-voltage.

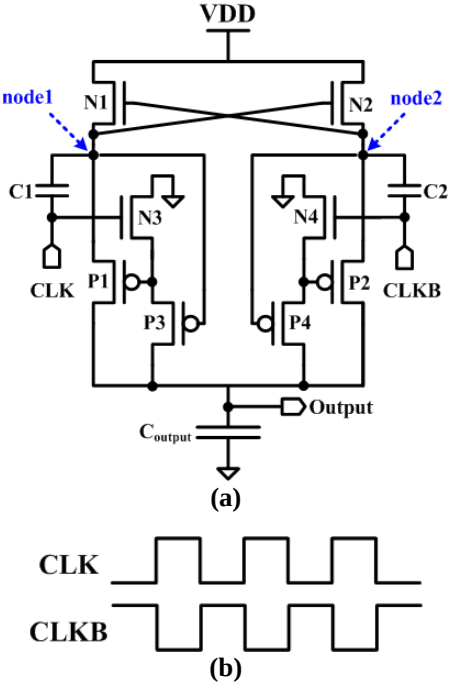

Fig. 2. The proposed DC-DC converter : (a) Schematic diagram and (b) Waveforms of input clock.

When the CLK signal becomes 'Low' and the CLKB signal becomes 'High', the node2 voltage changes from VDD to 2VDD, and the N1 TFT is turned on. As a result node1 voltage changes from 2VDD to VDD. The P3 TFT and the N4 TFT are turned on at the same time. This operation principle is symmetrical as explained in the case of the opposite phase of the clock signals. As a result, the proposed circuit has the advantage of decreasing the on-resistance of driving TFTs and also increasing the efficiency by making the gate voltage of driving TFTs have range from 0 to 2VDD.

4. Simulation results

We simulated the performance of the previously reported and the proposed circuits using HSPICE. We assumed that the load current is 120μA, input and output voltages are 5V and 9V, respectively. And the display system is assumed to 2.2 inch TFT-LCD with qVGA resolution format. Figure 3 shows the simulated gate voltage waveforms of driving TFTs of the previously reported and the proposed circuits. Figure 4 shows the simulated output voltages of the previously reported and the proposed circuits. If the two circuits are set to have the same output voltage, the size of the driving TFT of the proposed circuit is decreased by one sixth of the previously reported one. By lowering the gate voltage of driving TFTs, the driving capacity becomes increased, the size of the driving TFT can be decreased and the coupling capacitor can be small.

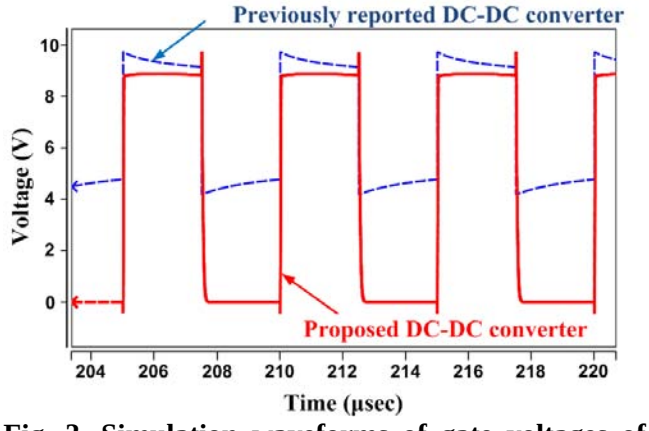

Fig. 3. Simulation waveforms of gate voltages of driving TFTs which are correspond to previously reported and proposed DC-DC converters.

Figure 5 shows the layout area of the previously reported and the proposed circuits. As shown in the figure 5, the area of the proposed circuit was decreased by 19% with respect to the previous one. Table 1 compares the efficiency of previous circuit and proposed circuit which are obtained by simulation. As shown in Table 1, the efficiencies of the previous and the proposed ones are 88.1% and 89.4%, respectively. Our simulation also reports that the output ripple voltage of the proposed circuit is 60mV while that of the previous one is 80mV.

TABLE 1. Simulation results of the proposed DC-DC converter and previously reported DC-DC converter

	Previously reported circuit	Proposed circuit
Output voltage	8.86V	8.87V
Ripple voltage	80mV	60mV
Area	100%	81%
Efficiency	88.1%	89.4%

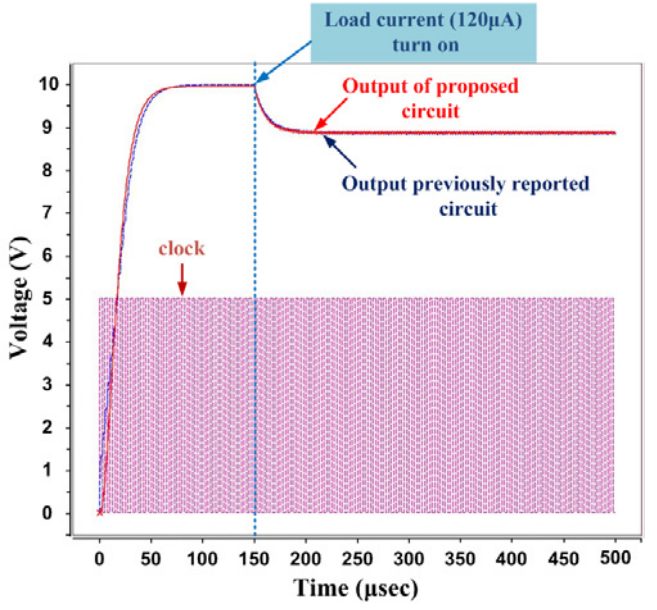

Fig. 4. Simulated waveforms of previously reported and proposed DC-DC converters.

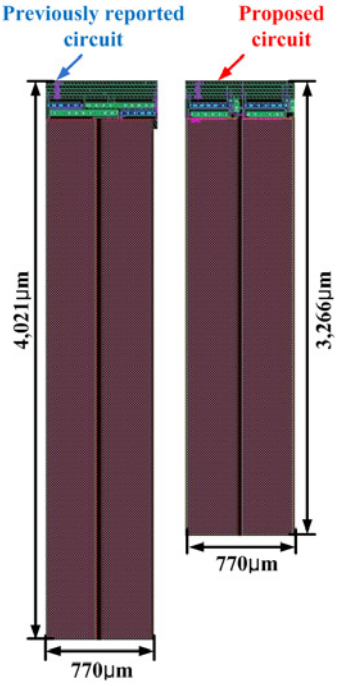

Fig. 5. Area comparison of previously reported and proposed DC-DC converters.

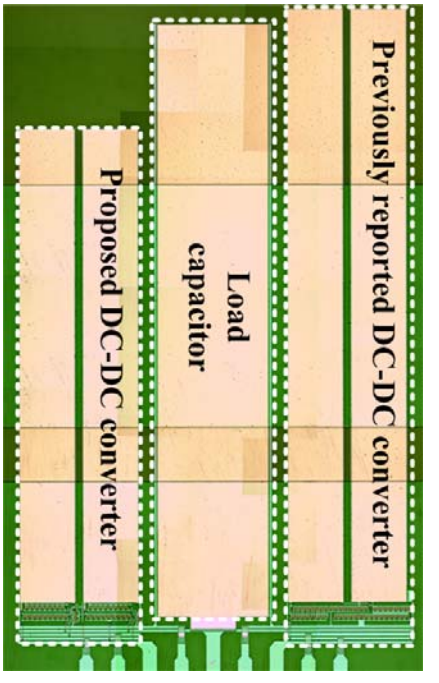

Fig. 6. Micrograph of previously reported and proposed DC-DC converters.

5. Measured results

The proposed DC-DC converter was implemented in 2-μm LTPS process. Figure 6 shows the micrograph of the fabricated previously reported and proposed DC-DC converters. Figure 7 shows measured waveforms of input and output of previously reported circuit and proposed circuit. The input clock voltage swings 5V and its frequency is 200KHz. When the load current is not consumed, the output voltage of previously reported one and proposed one are 10.22V and 10.2V, respectively. On the contrary, when the load current is consumed, the output voltages of each circuit are 9.28V and 9.352V, respectively. Measured efficiency of the previous one is 92.1% and the proposed one is 92.9%.

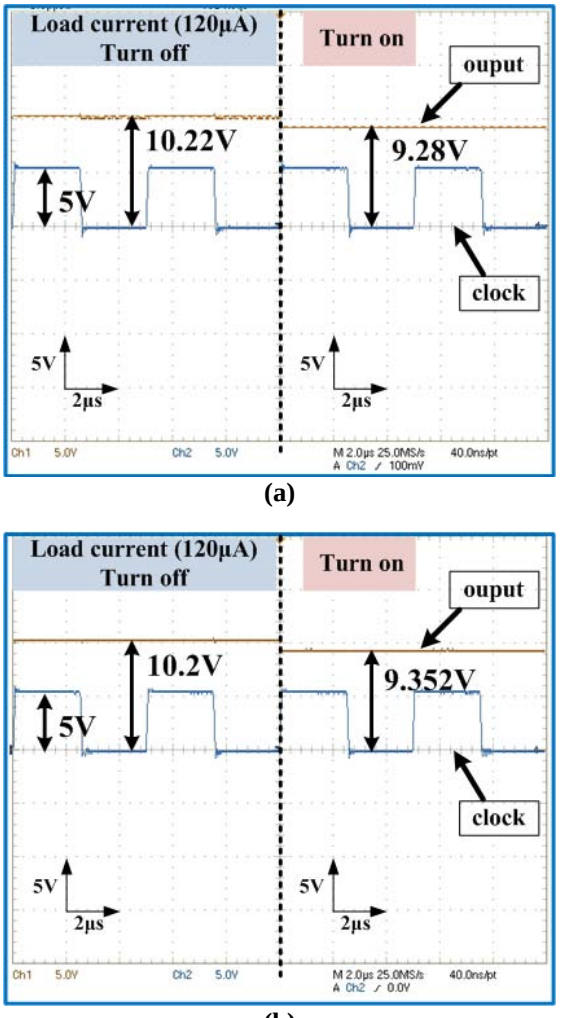

Fig. 7. Measured waveforms : (a) previous DC-DC converter and (b) proposed DC-DC converter.

TABLE 2. Measured results of previously reported DC-DC converter and proposed DC-DC converter

	Previously reported circuit	Proposed circuit
Output voltage	9.28V	9.35V
Area	100%	81%
Efficiency	92.1%	92.9%

6. Conclusions

We proposed DC-DC converter that has high efficiency and small area. Previously reported DC-DC converter has a disadvantage of the gate to source voltage of driving TFT being generally small. The proposed DC-DC converter overcomes that drawback of the previous one by lowering on-resistance of driving TFTs by means of making the gate to source voltage of driving TFTs large. Therefore, highly efficient and small area DC-DC converter using LTPS technology can be achieved. This also satisfies the needs of specification for mobile technology such as low cost, low power consumption, and compact size.

7. Acknowledgements

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8. References

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