A Study on Negative Bias Temperature Instability in ELA Based Low-Temperature polycrystalline Silicon Thin-Film Transistors

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Abstract

Negative Bias Temperature Instability (NBTI) in Eximer Laser Annealing (ELA) based Low Temperature polysilicon (LTPS) Thin-Film Transistors (TFT) was investigated. Even though NBTI is generally appeared in devices with thin gate oxide, the TFT with gate oxide thickness of 120 nm, relatively thick, also showed NBTI effect and dynamic NBTI effect is dependent on operational frequency.

1. Introduction

For applications such as system-on-panel (SOP), low-temperature polysilicon TFTs have recently been extensively studied for the fabrication of pixel, drivers, digital-to-analog converters (DACs) and timing controllers [1, 2]. Thus, their reliability has a direct impact on the product lifetime. NBTI has been widely studied and was found to be one of the most important reliability issues for the pMOSFETs. Although much work related to NBTI has been done on MOSFET with single crystal, few works have been done on polysilicon TFT. In this study, NBTI in Eximer Laser Annealing (ELA) based LTPS TFTs was investigated and estimated how much this degradation affects device performance.

2. Experimental

We used glass substrate with a SiO_2 buffer layer to fabricate low-temperature polysilicon (LTPS) TFTs, First, amorphous silicon films were deposited on the glass substrates by plasma-enhanced chemical vapor deposition (PECVD). Then, excimer laser annealing was utilized to crystallize an amorphous film (50 nm) for a low temperature process followed by polysilicon active area patterning. Subsequently, a gate-oxide layer (SiO_2, 80 nm thick) was formed by PECVD. at a substrate temperature of 350^{o}C. In addition to the silicon dioxide layer, an interposed silicon nitride (SiN_x) film was deposited to prevent the incorporation of mobile ions into the SiO_2 gate insulator. The SiN_x layer was 40 nm thick and was deposited at a substrate temperature of 430^{o}C. The n^+ regions were created by plasma ion doping. A gate metal (Mo) was then formed. A dielectric layer was deposited by PECVD. Subsequently, dopant activation was carried out thermally. Contact hole were formed, and a source drain metal was deposited and patterned. A passivation layer was deposited and patterned to complete the fabrication process. All the processes were carried out in a class-10 clean room with minimum direct human contact. The gate dielectric thickness was varied to investigate how this thickness affects NBTI. The frequency dependence of NBTI was also investigated.

3. Results and discussion

Fig. 1 shows the NBTI stress arrangement. Fig. 2 shows the threshold voltage shift with increasing negative gate bias stress time. NBTI of gate length dependency was also performed. It is well known that the threshold voltage shift of MOSFET under NBTI shows a power-law dependence on stress time with an exponent factor of 1/4-1/3, which can be illustrated by

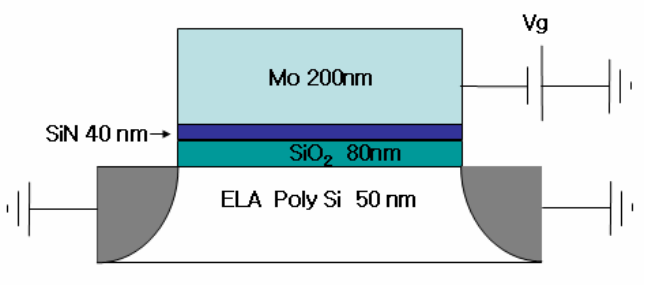

Fig. 1. Schematic diagram of NBTI

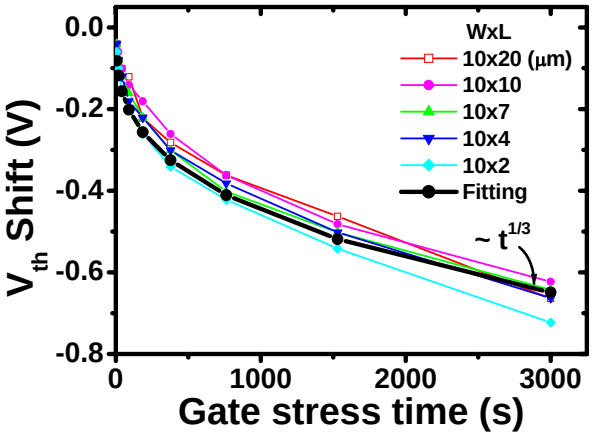

Fig. 2. Theshold voltage shifts as a function of stress time.

the diffusion-controlled electrochemical reactions. In the measured data shown in Fig. 2, the fitted value is 1/3, which is well agreement to the reported value [3]. Generally, NBTI is appeared in pMOSFET with thin gate oxide due to the generation of fixed oxide charges and interface states during negative gate bias stress, resulting in the threshold voltage shift [4]. In this experiment of static NBTI (SNBTI), despite the thick gate oxide thickness of 120 nm, the threshold voltage shift was measured to -0.6 V after stress of gate voltage of – 20V at 200°C for 3000 s. However, the observed NBTI was not dependent on gate length. From these results we concluded that the amount of boron penetration from source and drain to gate oxide is negligible [4]. Fig. 3 shows the estimation of the effects of NBTI in OLED load line. The marked two 'X' points indicate the corresponding degradation of on current after NBTI which will deteriorate OLED luminance significantly. Fig. 4. shows the breakdown electric field of TFTs for two different gate oxide thickness. The TFTs with thicker gate oxide shows higher breakdown field.

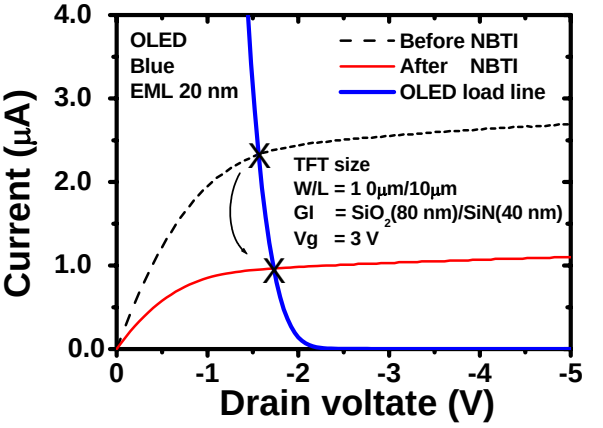

Fig. 3. Effects of SNBTI on load line-p-type LTPS TFT V_DI_D & OLED load line.

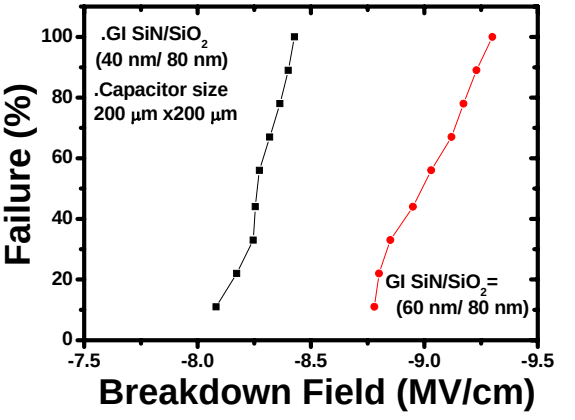

Fig. 4. Breakdown electric field for two different gate oxide thicknesses

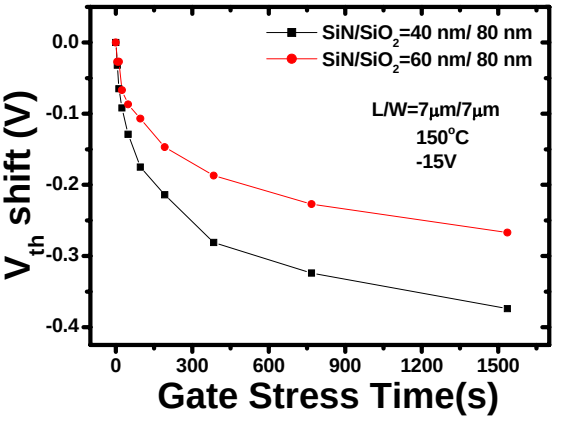

Fig. 5. Threshold voltage shift as a function of stress time for two different gate oxide thick

This behavior is believed to the different rate of generation of interfacial traps as the bias voltage increase for two different gate insulators. Fig. 5. shows the threshold voltage shift as a function of stress time for two different gate oxide thicknesses. The TFT with thicker gate oxide shows less threshold voltage shift. The TFT with thicker gate oxide undergoes relatively less electric field compared to that with thinner gate oxide thickness, which leads to less generation of interfacial state. According to the standard static reaction-diffusion model Si:H interacts with holes accumulated in the inversion layer during NBTI stress, and then the accumulated holes weaken the Si:H bond and create interface traps by releasing the hydrogen species (atom, molecule or ion) at the Si/SiO_2 interface. Initially, the generation of interface trap depends on the rate at which the Si:H can be dissociated. Later the diffusion of hydrogen becomes the rate limiting step. This leads to power-law dependence on NBTI degradation [4]. However, recent dynamic (AC) NBTI tests show that the interface traps generated during on state of these transistors are partially annealed during their off state (electric passivation effect), thereby the predictions based on the SNBTI test, where the transistor is always on state, may be unduly pessimistic [5-7]. Some have claimed that the magnitude of NBTI is frequency independent [5], while others have demonstrated that the frequency dependence, although weak, is nonetheless important [6].

To investigate the frequency dependency of NBTI for polySilicon TFT, several sets of experiment with various frequencies was performed. Fig. 6 shows the both static (0 Hz) and dynamic NBTI of the fabricated pTFT in this experiment. The amplitude of the pulse shape utilized in this experiment was (10,-15V) at 150 ^{o}C. As the frequency of the stress bias is increased the shift of threshold voltage is reduced. This effect is known as electric passivation. Fig. 7. shows the corresponding generated D_{it} with increasing stress time. The amount of D_{it} is calculated from the following relation.

$$\Delta D_{it} = \frac{C_{ox}}{2.3kT}\left[\ \frac{1}{slope(after)} - \frac{1}{slope(before)}\ \right]$$

The amount of generated D_{it} is $1x10^{11}/cm^2$ and $5x10^{10}/cm^2$, for static (0 Hz) NBTI and 100 kHz, respectively. Even though the exact mechanism of DNBTI effect in polysilicon TFT is not yet understood

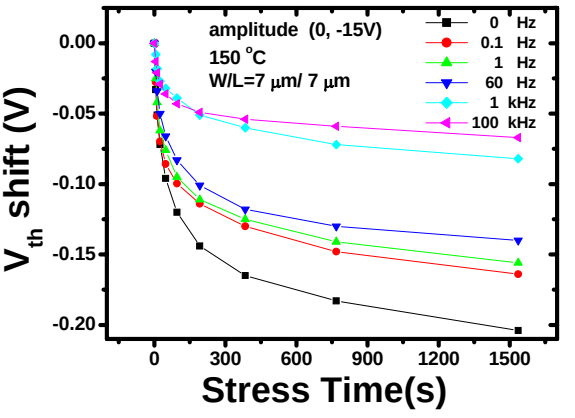

Fig. 6. Threshold voltage shift for various stress frequency.

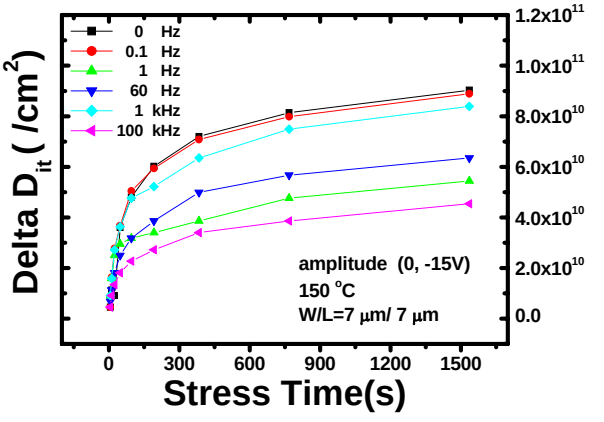

Fig. 7. Delta D_{it} calculated by swing for various frequency.

completely, the much shift of threshold voltage in SNBTI despite thick gate oxide is supposed to be related to many defects in the polysilicon bulk. The other factor is supposed to the low temperature comical vapor deposition (CVD) gate oxide which has poor interface between gate oxide and substrate polysilicon. From the results of NBTI experiment, we concluded that the reliability of ELA based p-type LTPS TFT should be enhanced by utilizing new gate oxide material or improving process technology. Thereafter we can make more reliable SOP system by utilizing polysilicon TFT.

4. Summary

NBTI effect of p-TFT was examined. Compared to

single crystal silicon MOSFET, TFT with relatively thick gate oxide thickness of 120 nm showed significant NBTI effect. The threshold voltage shift of p-TFT involving NBTI depends on operation frequency. We concluded that the reliability of ELA based p-type LTPS TFT should be enhanced by utilizing new gate oxide material or improving process technology. Thereafter we can make more reliable SOP system by utilizing polysilicon TFT

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