6 Mask LTPS CMOS Technology for AMLCD Application

Soo-Jeong Park, Seok-Woo Lee, Myoung Kee Baek, Yong Su Yoo, Chang Yeon Kim, Chang-Dong Kim, and In Byeong Kang

LCD R&D Center, LG.Philips LCD, 533, Hogae-dong, Dongan-gu, Anyang-shi, Kyoungki-do, 431-080, KOREA
Phone: +82-31-450-7470, E-mail: sjpark04@lgphilips-lcd.com

Keywords : LTPS, CMOS, AMLCD

Abstract

6Mask CMOS process in low temperature polycrystalline silicon thin film transistors (poly-Si TFTs) has been developed and verified by manufacturing a 6Mask CMOS AMLCD panel. The novel 6Mask CMOS process is realized by eliminating the storage mask, gate mask and via open mask of conventional structure.

1. Introduction

Active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light emitting diode (AMOLED) displays using low temperature poly-crystalline silicon thin film transistors (LTPS poly-Si TFTs) have attracted considerable attention due to their high current driving capability and integration of circuit[1][2]. However, poly-Si TFT has more complicated process than that of amorphous silicon (a-Si) TFT. Thus, in spite of having superior performance, poly-Si products are insufficiently competition on cost comparing with a-Si products. To be more competitive in the market, it is necessary to reduce photo mask steps of poly-Si process. Thus there has been much effort to reduce the number of mask steps in order to achieve the low-cost process [3][4][5].

In this paper, the development of a novel 6Mask CMOS technology, which is promising technology in terms of the competitiveness of poly-Si CMOS products, is introduced.

2. Experimental

Fig. 1 shows comparison of process sequence between conventional 9Mask CMOS process and proposed 6Mask CMOS process.

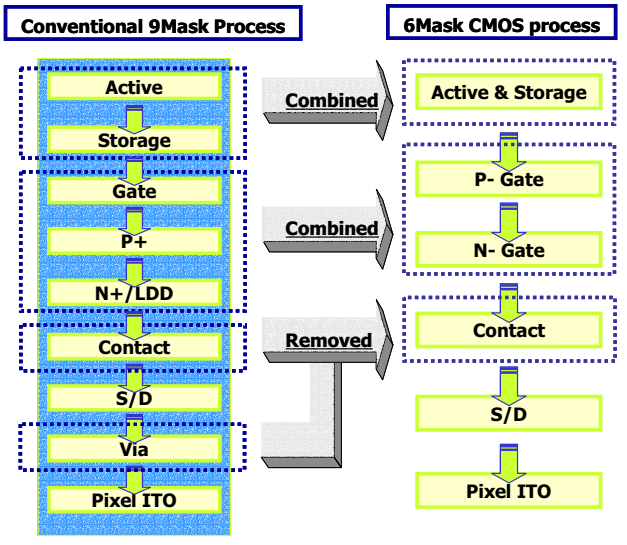

Fig.1. The comparison of the process sequence between proposed 6Mask CMOS poly-Si TFT and conventional 9Mask CMOS poly-Si TFT

Comparing conventional 9Mask CMOS process, the 3-photo mask steps were reduced; i.e., storage doping mask, gate mask and via open mask.

6Mask CMOS poly-Si TFTs was fabricated using low temperature coplanar process. Firstly, stacked SiN_x and SiO_2 buffer layers were deposited sequentially on a glass substrate by plasma enhanced chemical vapor deposition (PECVD) to suppress mobile charge diffusion from glass substrate. The thickness of dehydrogenated precursor PECVD amorphous silicon was 50 nm. Dehydrogenation process was carried out over 430℃ in nitrogen ambient. Then, poly-Si layer with average grain length of 2 ㎛ was crystallized by sequential lateral excimer laser irradiation with laser energy density over 1000 mJ/cm^2.

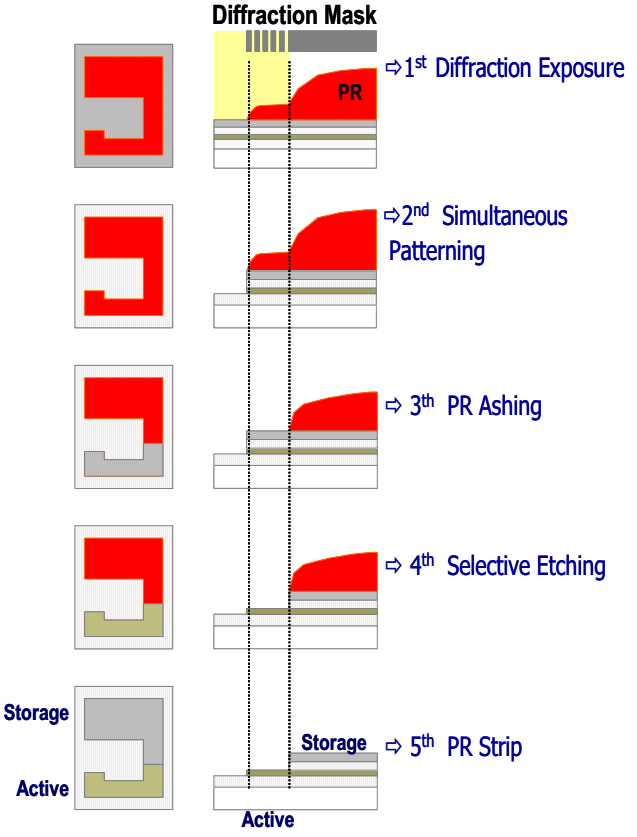

Fig.2. The process flow of the active & storage doping mask step using diffraction exposure

(a)

(b)

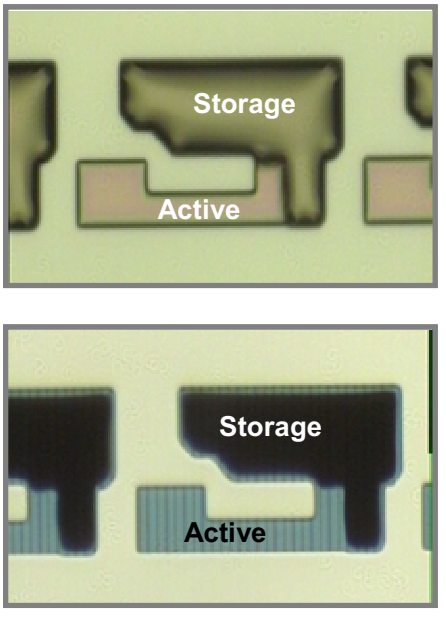

Fig.3. The microscope images of active and storage area (a) after diffractive exposure and (b) after PR strip process in TFT area

In order to simultaneous patterning of active and storage, SiH_4-based 1st gate oxide deposition on poly-Si was followed by storage metal sputtering. Fig. 2 shows the process flow of the active and storage doping mask step using diffraction exposure as the one of the key process in the proposed structure. In the first step, the active and the storage capacitor regions were simultaneously patterned by diffractive exposure. And then photo resister (PR) was slightly ashed to selectively remove PR only on the diffractive area. And storage metal was removed in TFT area by selective etching process.

Fig. 3(a), (b) show the microscope images of active and storage area (a) after diffractive exposure and (b) after PR strip process in TFT area. The storage metal was remained only on the storage area shown as Fig. 3(b). After simultaneous patterning of active & storage region, 2nd gate oxide and gate metal were successively deposited. P-gate and N-gate regions were selectively defined using respective doping mask, i.e., P-gate patterning was followed by P+ doping, and then N-gate patterning was also followed by N+ doping. Considering the layout of 6Mask structure, only the overlapped common area of each photo mask step remained to the end of the process. LDD region was defined by gate CD loss in N-TFT and it had gradual doping profile. After respective gate patterning and doping, a 100 nm-thick interlayer was deposited and thermally activated. And a 700 nm-thick passivation layer was deposited after activation, and thermal annealing was applied to improve hydrogenation efficiency. After double interlayer open, source/drain(S/D) data metallization and patterning was followed. Finally, ITO was directly patterned on S/D layer with covering all S/D metal region to avoid galvanic corrosion of S/D metal during ITO etch step.

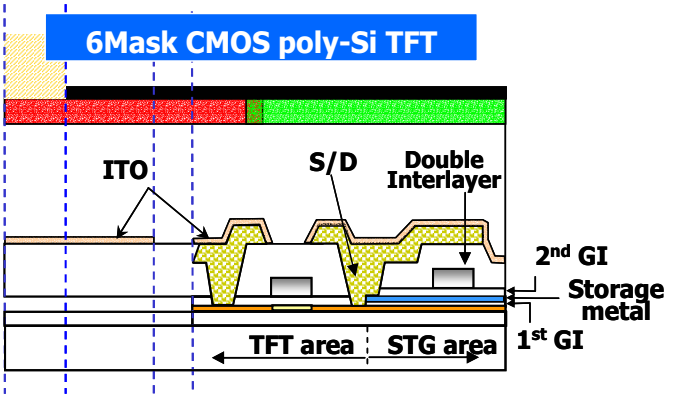

Fig.4. The cross sectional view of the proposed 6Mask CMOS structure

Fig. 4 shows the cross sectional view of proposed 6Mask CMOS structure. Storage metal inserted between the storage common electrode and the active layer was creatively substituted for storage doping layer which was required to reduce the resistance of the active layer used as a storage capacitor for line inversion operation without an additional mask step.

3. Results and discussion

3.1 Electrical Characteristics

Fig. 5(a), (b) shows the transfer characteristics of the 6Mask CMOS poly-Si TFTs of N- and P-type, respectively. Both N-and P-type TFTs revealed excellent transfer characteristics. The on/off current ratio, the field effect mobility, and the S-factor of N-type TFT were ~10^8, ~226cm^2/Vsec, and 0.259V/dec, respectively. In case of the P-type TFTs, they were ~10^8, ~111cm^2/Vsec, and 0.223V/dec, respectively. V_{th} range was around 1.2V regardless of TFT types, which showed less than 10% of uniformity within the glass. The performances of 6Mask CMOS devices were almost same, but higher current drivability than 9Mask CMOS devices.

3.2 Verification of 6Mask CMOS Technology

6Mask CMOS technology was successfully verified by manufacturing CMOS panel with 6Mask process. 6Mask-process-based layout revision was carried out on 6.94-inch WVGA CMOS poly-Si panel with integrated driver including sequential analog sampling circuit as introduced elsewhere [6]. Table 1 describes the spec. and feature of the 6.94-inch WVGA panel. Fig. 6 shows the image of 6Mask CMOS panel, which reveal image quality equal to 9Mask CMOS panel.

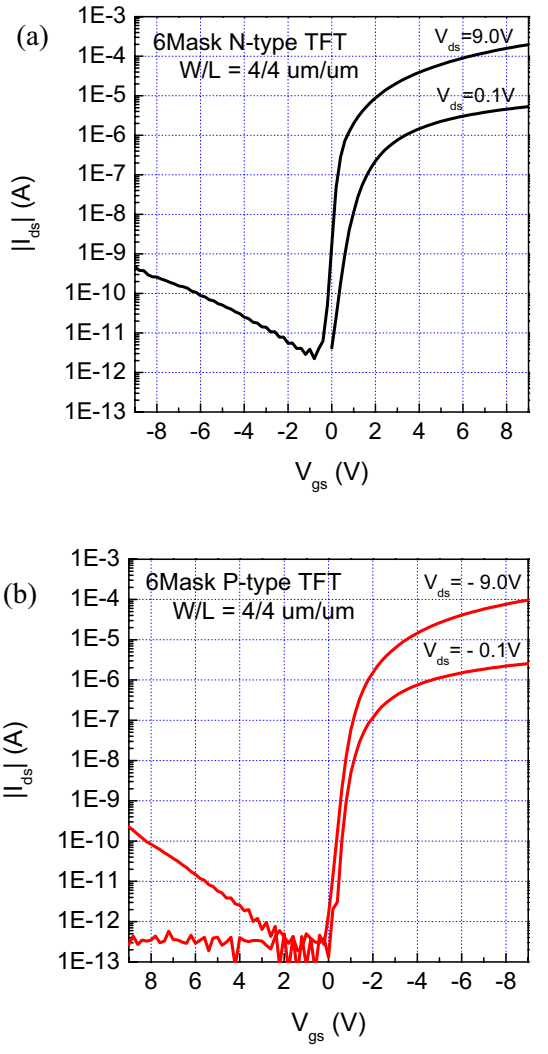

Fig.5. The electrical characteristics of (a) N- (b) P-type TFT using 6Mask CMOS process with W/L =4/4μm

4. Conclusion

Novel 6Mask CMOS structure suitable for panel operation with line inversion was developed by eliminating the storage mask, gate mask and via open mask of conventional structure. And we successfully verified by manufacturing 6.94-inch WVGA (800×480) AMLCD panel with integrated circuit. The competitiveness of CMOS product will be strengthened in the market by adopting 6Mask CMOS process.

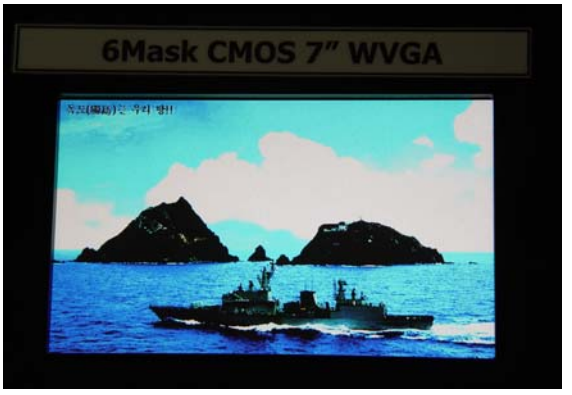

Fig.6. The panel image of 6.94-inch WVGA AMLCD using the proposed 6Mask CMOS process

Table 1. The spec and features of 6.94-inch WVGA panel

Parameter	Spec. & Features
Display size	6.94 inch
Resolution	800×RGB×480 [16:9]
Sub-pixel pitch	63(um)(H) ×189(um) (L) [WVGA]
Integration	-Gate Driving circuit -Data De-multiplexing circuit -Gate Driver Logic Redundancy

5. References

[1] K. Kanzaki., Dig Tech. Papers, AMLED, **p71, 200 1**

[2] C. H. Kim, I.H. Song, M.K. Han, "A New High Performance Poly-Si TFT by Simple Excimer Laser Annealing on Selectively Floating a-Si Layer", IEDM 01, **pp. 751-754, 2001**.

[3] C. Yi, P.-M. Choi, U.-S. Kim, D.-B. Kim, C.-W. Kim, K. Chung, "Development of CMOS Six Mask and PMOS Five Mask Poly-Si Architecture with RGB+White Color," SID Diges, Vol. 35, **pp. 229-231, 2004**.

[4] Norbert Fruhauf, "LTPS processes of AMLCD and AMOLED Applications," SID Diges, Vol38, **pp.69-72, 2007.**

[5] Y.I Park, "LTPS PMOS Four-Mask Process for AMLCDs," SID Diges, **pp341-343, 2005.**

[6] Kyoung Moon Lim, et al., "A 6.94-in. WVGA Poly-Si TFT-LCD with Integrated Driver Including Sequential Analog Sampling Circuits," Displays 27, **pp. 191-196, 2006**.