Electrical instabilities in p-channel polysilicon TFTs: role of hot carrier and self-heating effects

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Abstract

The effects of hot carriers and self-heating on the electrical stability of p-channel TFTs have been analysed combining experimental data and numerical simulations. While hot carrier effects were shown not to induce appreciable degradation, self-heating related instability was found to more seriously affect the device characteristics. New models have been developed to explain the reported results.

1. Introduction

Low-temperature polysilicon (LTPS) Thin Film Transistors (TFTs) have been widely applied to active matrix liquid crystal displays (AMLCD) and active matrix organic light emitting displays (AMOLED). Recently, the decrease of maximum process temperature allowed the application of LTPS TFTs as driving transistors in AMOLED displays on flexible metal and polymeric substrates. These applications require very reliable devices and p-channel LTPS TFTs are to be preferred, as they are less influenced by hot carrier effects (HCE) than n-channel TFTs [1,2]. Indeed no degradation of the transfer characteristics has been observed under bias stress in the hot carrier regime and even an apparent improvement of the field effect mobility, μ_{FE}, has been reported [1]. However, when operating the p-channel devices at high gate and drain voltages, so that drain current is large enough to induce appreciable self-heating of the device, degradation of the electrical characteristics is normally observed [3].
The on-current increase, induced by HCE, has been explained by hot electron trapping into gate oxide near drain contact, inducing channel shortening [1]. The self-heating related instabilities can be related to the well known negative bias temperature instability (NBTI) effect [4], commonly observed in p-channel c-Si MOSFETs [5,6]. NBTI in c-Si MOSFETs is attributed to the generation of interface traps and fixed oxide charge [5,6]. The generation mechanism is related to the breaking of the passivated Si-H bonds at the Si/SiO_2 interface, leading to donor-like interface traps. The bond breaking can be induced by the holes accumulated at the interface captured by the Si-H bonds [5]. However, several other breaking mechanisms have been suggested [7], involving hydrogen and/or water related species (H_2O, OH^-, etc.). In polysilicon TFTs, it has been also proposed [4] that NBTI is related to both grain boundary traps and interface state generation.
In order to clarify the HCE and NBTI effects in p-channel polysilicon TFTs, we analysed the experimental measurements using two-dimensional numerical simulations.

2. Experimental

Polysilicon thin films transistors have been fabricated using as active layer precursor a-Si film, deposited by PECVD to a thickness of 80 nm and laser crystallized by XeCl excimer laser, obtaining polycrystalline active layer with typical grain size in the range of 0.4 - 0.8 μm. Silicon dioxide (100 nm), deposited by PECVD, was used as gate insulator. Gate electrode (Al-film, 300 nm thick) was used as implantation mask for boron ion implantation, obtaining a self-aligned (SA) source-drain contacts.
In order to test the hot-carrier induced degradation, we performed bias-stress experiments applying V_g slightly above the threshold voltage, where the hot-carrier degradation is expected to be maximum (see ref. [1]), and large V_{ds}. In particular, the electrical stability of p-channel TFTs was tested by sequentially bias-stressing for $4x10^3$ s with gate

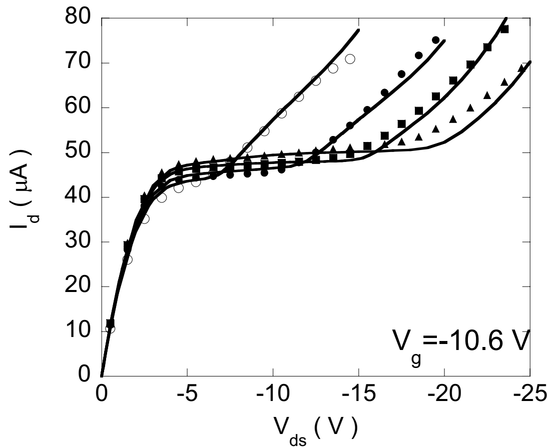

Fig.1:Experimental (symbols) and simulated (lines) output characteristics of p-channel TFT measured before (open circles) and after sequential bias stressing for 4 x 10^3s with gate voltage $V_{g\ stress}$=-10,6V and decreasing drain voltage $V_{d\ stress}$=-15V (closed circles), -20V (squares), and -25V (triangles).

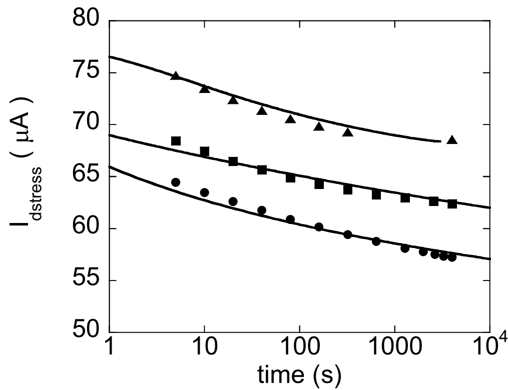

Fig.2: Experimental (symbols) and simulated (lines) drain current measured during bias stress at each cycle at V_g=$V_{g\ stress}$ and V_d=$V_{d\ stress}$ [$V_{d\ stress}$=-15V (circles), -20V (squares), and -25V (triangles)].

voltage, $V_{gstress}$=-10.6 V and increasing drain voltage, $V_{dstress}$ =-15 V, -20 V and -25 V. Both transfer (measured at V_{ds}=0.1V) and output (measured at V_g=$V_{gstress}$) characteristics were monitored at selected times during the bias-stressing cycles. After bias stress, minor changes were observed in the transfer characteristics, with a slight increase in the on-current, in agreement with what already reported in the literature [1]. On the contrary, relevant variations have

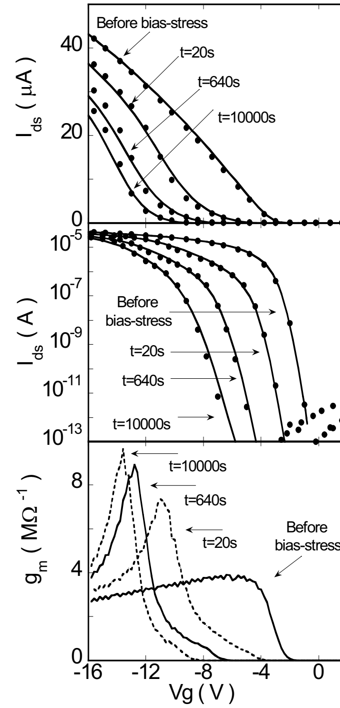

Fig.3: Experimental (●) and simulated (solid lines) transfer characteristics, measured at different times of bias stress with V_{ds}=-0.1V, in the linear and logarithmic scale for a SA device with channel width W=50µm and channel length L=6µm. Bias stress conditions: V_g=-15 V , V_{ds}=-11V. Also shown are the transconductance, g_m, vs gate voltage, V_g, for different bias stress time.

been observed in the output characteristic, shown in fig.1. In particular, before bias-stressing for V_{ds}<-6V an anomalous drain current increase appears, usually referred as kink-effect [8] and related to impact ionization occurring near the drain and enhanced by the parasitic bipolar transistor effect [8]. As can be seen from Fig. 1, the kink-effect is progressively reduced after each bias-stress cycle for increasing negative $V_{dstress}$ and the onset appears shifted to more negative V_{ds}. In addition, the saturation current after each bias-stress cycle slightly increases, in agreement with the on-current increase observed in the transfer characteristics. In fact, by using the model reported in ref. [9], it was possible to reconstruct the output characteristics starting from the transfer characteristics measured after bias stress and we could confirm that the saturation current increase was simply due to the effective channel length reduction. The drain current, measured during bias-stress at each

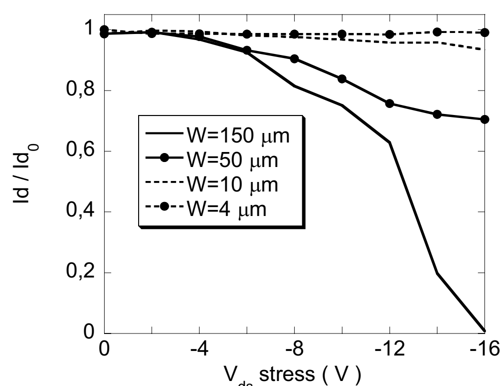

Fig.4: The relative on-current variation, measured at V_g=-15V and V_{ds}=-0,1V, vs bias stressing V_{ds} for a SA device with same channel lenght L=6μm and different channel width W. Bias stress conditions: V_{gs}=-15V while V_{ds} was incremented in step of 2V every 60s.

cycle at $V_{gstress}$=-10.6 and the corresponding $V_{dstress}$, monotonically decreases as shown in Fig. 2.

To test the electrical stability in the self-heating regime we performed bias-stress experiments with Vg-Vt=-12.5 V and Vds=-11V, in order to induce appreciable joule heating of the device, and for t up to 10000 s. In Fig. 3 the transfer characteristics are reported during the bias-stress experiment, showing a threshold voltage increase (in modulus) and subthreshold slope degradation induced by bias-stress. In addition, μ_{FE} shows an apparent increase induced by the bias-stress, as evident from the bottom panel of Fig. 3, where the transconductance (gm) is reported. Indeed, from Fig. 3 we can evaluate an apparent increase in μ_{FE} from 88 cm^2/Vs to 220 cm^2/Vs. The present results clearly show that a substantial degradation appears when the devices are operated under high gate and drain bias conditions. For such operation conditions self-heating is expected to occur [10] and device degradation appears very sensitive to temperature. This is confirmed by the dependence upon device geometry of the device degradation. In fact, it has been recently shown for n-channel polysilicon TFTs fabricated on glass, biased with same conditions, that decreasing channel width, W, leads to a decrease of the temperature in the central region of the channel [10], as a result of the increased weight of the lateral heat dissipation and the relatively low vertical heat flux towards the substrate. Indeed, when performing accelerated stability test in devices with different channel width, W, and same channel length, L, the on-current variations, measured in a SA device at Vg-Vt=-12.5 V and Vds=-0.1V and reported in Fig 4, show that devices with small W are quite stable, up to -16 V Vds, while the on-current starts to be seriously degraded for Vds< -5V for larger W.

3. Numerical Simulations

First we analysed the hot carrier induced degradation, shown in Figs. 1 and 2, where bias stress experiments are performed in the kink effect regime of the output characteristics. It is well known that hot-carrier induced degradation in p-channel c-Si MOSFET, operating in the kink effect regime, is related to trapping of injected electrons into pre-existing oxide traps or newly generated traps, induced by hot electron injection [11-13]. Hot electron injection in p-channel devices is triggered by the avalanche multiplication [11-13] taking place at the drain end of the channel, where impact ionisation is stronger [8]. To localise the effects induced by hot-carriers, we modelled the hot-electron trapping assuming a predominance of pre-existing oxide traps [12, 13], with an areal density N_{T0}, and by using a simple first order rate equation for the capture of electrons into the oxide traps [11]:

$$\frac{dN}{dt} = \sigma_e J_e \left(N_{T0} - N \right) / q \qquad (1)$$

where N is the trapped electron density, σ_e is the capture cross section of the oxide traps and J_e is the hot electron current injected at both front and back interfaces into the gate and substrate dielectrics, respectively. J_e has been computed according to the expression proposed by Hofmann et al. [14], using a lucky-electron approach [15]. The carrier density and electric field distributions needed in order to compute the carrier injection currents are derived employing a 2-D device numerical simulation program such as DESSIS [16]. To determine in a self-consistent way the spatial and time evolution of the interface state and oxide trapped charge distributions, these quantities are computed using the following iterative generation algorithm: starting with the simulation where no interface states and trapped charges are present, distributions are evaluated along the front and back interfaces. Then, the equation (1) is solved on time interval δt assuming that the J_e distributions do not change significantly during this time. The resulting trapped charge distributions are then introduced in the simulation and the characteristics are re-evaluated, obtaining a new hot-carrier injection

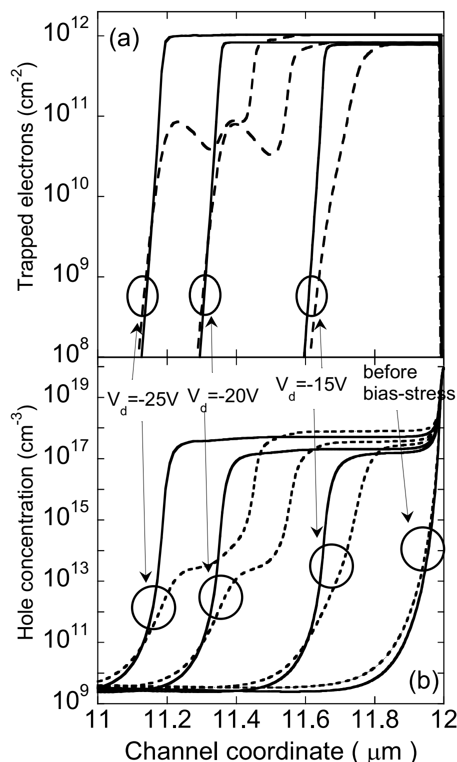

Fig.5: Trapped electron distributions (a) and positive charge concentration in the channel (b) at the front (solid lines) and back (dashed lines) interfaces, calculated after bias stressing for 4000s with three different conditions, as indicated.

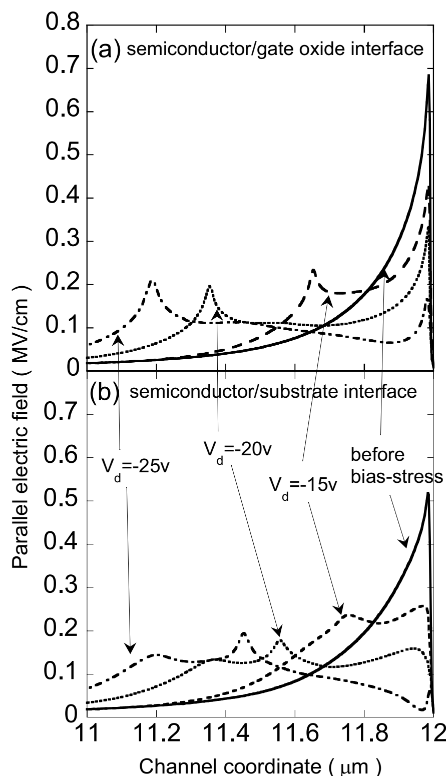

Fig.6: Electric field, parallel to the hole current, calculated at the front (a) and back (b) interfaces after bias stressing for 4000s with three different conditions, as indicated.

current distribution, which is then used for the next algorithm iteration step.

The sequential bias-stress experiment performed with increasing $V_{dstress}$ was then reproduced by using the above described model. In particular, we first run the simulated bias-stress at $V_{gstress}$=-10.6 and $V_{dstress}$=-15 V for 4000 s and then we determined the trapped electron density distributions at both front and back interfaces (see Fig. 5a). By using these distributions the output characteristics were re-evaluated and the simulated characteristics are reported in Fig. 1. Starting now with the resulting distribution after this first stage we run the second simulated bias stress by incrementing the $V_{dstress}$ to –20V and obtained after 4000 s new distributions for the trapped electrons (see Fig. 5a). Same procedure was used for the third and final bias-stress cycle at $V_{dstress}$=-25 V. The trapped electron distributions show that the region where trapping occurred is progressively expanding (up to 0.8 µm) as the $V_{dstress}$ was decreased. Furthermore, to properly fit the experimental data we found that it was necessary to increase the N_{T0} value, from $7.8x10^{11}cm^{-2}$ for the first cycle to $8.3x10^{11}$ cm^{-2} for the second cycle and to $10.3x10^{11}$ cm^{-2} for the last cycle. This implies that by increasing $V_{dstress}$ an increased number of pre-existing oxide traps become available for trapping events. We note that by increasing $V_{dstress}$ electrons can gain more energy and, therefore, can be injected deeper into the gate oxide. As a result, electrons can be trapped into states at increasing distances from the oxide/semiconductor interface, thus increasing the effective areal density N_{T0}. In Fig. 2 the simulated time variation of the drain current vs bias stress time is compared with the experimental data for each bias-stress cycle and a very good agreement is found.

By using the trapped electron distributions shown in Fig. 5a transfer (not shown) and output characteristics after bias stress were simulated and a very good agreement with the experimental data is obtained, including the saturation current increase (see Fig. 1). The slight on-current increase (2.2%, 3.45%, and 4% after each of the three bias-stress cycles) was also well reproduced (simulated on-current increase of 1%, 2% and 3%, respectively). It should be pointed out that by assuming that the observed on-current increase is due

to channel shortening [1], with the effective channel length being $L_{eff}=L-\Delta L$, and considering as ΔL the extension of the region near the drain where electrons are trapped, we should expect a much higher (8% for the last cycle, for instance) on-current increase than effectively observed (4%). This is due to the relatively moderate number of trapped charge density ($<10^{12}$ cm^{-2}), which induces a p^- region near the drain (see fig 5b), that can be modulated by applied gate voltage, making the estimate of the effective channel length not straightforward.

The formation of a p^- region near the drain junction explains the reduction of kink effect observed during bias stress experiments. Indeed, the reduction of the abruptness of the channel/p^+ junction decreases the electric field parallel to the current flow, as shown in fig. 6, at both back and front interfaces, thus reducing the impact ionization rate. In addition, fig. 6 shows that the presence of injected charge modifies the electric field distribution. At the front interface, after bias-stress, two peaks are observed, located at the drain junction and at the edge of injected region (fig. 6). The first peak is progressively reduced for increasing $V_{dstress}$, whereas the intensity of the second peak remains almost constant corresponding to an almost constant injected charge density. At the back interface the electric field shows a more complex behavior and a third peak can be observed for $V_{dstress}$=-20V and –25V, corresponding to the peaks of injected charge located at x=11.4 μm and 11.2 μm, respectively (see fig. 5a).

Two dimensional numerical simulations were also employed to analyse the observed device instability in the self-heating regime. In p-channel c-Si MOSFET the high temperature and high gate voltage operations induce interface state generation and charge trapping, that shift the transfer characteristics increasing subthreshold slope and decreasing the flat band voltage [5, 6]. Therefore, in analogy to c-Si p-channel MOSFETs [5], we assumed that NBTI induces a uniform distribution along the channel of interface states and oxide fixed charge. On the other hand, in the case of SA LTPS TFTs, we note that the on-regime is characterized by a gm increase (see Fig. 3), induced by the bias stress, which is rather difficult to be explained in terms of either charge injection or interface states formation along the channel. In addition, an explanation of the gm increase in terms of channel shortening effect [1] can be also discarded, on the basis of the bias stress experiments performed at low Vds.

From previous analysis, using numerical simulations, we showed that similar gm increase can be related to the formation of interface states and/or charge trapping into the gate oxide in a narrow channel region near the source and/or drain contacts [17]. Therefore, to explain the modifications of the electrical characteristics, presented in Figs. 3 and 4, we assumed that, in addition to the formation of interface states and oxide fixed charge along the channel, extra defects are generated at the gate edge regions, whose extension was fixed to 100 nm. According to this scheme, the resulting TFT characteristics are determined by the series of three TFTs, with the two TFTs at the gate edges having a different flat-band voltage from the central TFT. By using appropriate interface state and fixed charge densities in the channel and at the gate edge regions, it was possible to perfectly reproduce the degradation observed, as shown in Fig. 3. In particular, we adopted a gaussian distribution for the donor-like interface states, centered at 0.2 eV from the valence band and with a width (standard deviation) of 0.1 eV, and by using different values of the maximum interface state density (Nss) and of the oxide fixed charge (Nox), as reported in table I, it was possible to perfectly reproduce the different curves obtained during bias stress (see Fig. 3). It is very interesting to see from Fig. 3 that the simulations correctly predict the apparent field effect mobility increase, as experimentally observed. The gm overshoot arises from the interplay between the central and lateral TFTs: for low Vg, the resistivity of the two defected regions at the gate edges dominates the channel resistivity while at high Vg, the on-current is again limited by the central transistor. The apparent gm increase coincides with the transition between these two regimes. We note that the apparent field effect mobility enhancement could be hardly reproduced using a different approach not including the positive charge build up in the two narrow regions at the gate edges.

Tab.I

Stress Time	**t=20s**	**t=640s**	**t=10000s**
N_{ss} channel	**$0.12x10^{12}cm^{-2}eV^{-1}$**	**$0.24x10^{12}cm^{-2}eV^{-1}$**	**$0.2x10^{12}cm^{-2}eV^{-1}$**
N_{ox} channel	**$0.62x10^{12}cm^{-2}$**	**$1.29x10^{12}cm^{-2}$**	**$1.7x10^{12}cm^{-2}$**
N_{ss} Gate edge	**$7.0x10^{12}cm^{-2}eV^{-1}$**	**$6.0x10^{12}cm^{-2}eV^{-1}$**	**$4.0x10^{12}cm^{-2}eV^{-1}$**
N_{ox} Gate edge	**$1.3x10^{12}cm^{-2}$**	**$2.3x10^{12}cm^{-2}$**	**$3.1x10^{12}cm^{-2}$**

Tab.I: Interface state density (maximum value of the gaussian distribution), N_{SS},, and oxide fixed charge density, N_{ox}, for the channel and Gate edge regions after different bias-stress times.

We therefore attribute to this aspect of the electrical characteristics degradation a crucial significance and it represents the fingerprint that the variations are not occurring uniformly along the channel. The enhancement of NBTI at the gate edges can be related to several mechanisms. The gate oxide as well as the Si/SiO_2 interface at the gate edges are damaged by ion-implantation and could not be fully recovered by the post-implantation laser annealing. Defects at interface are passivated by forming gas annealing, generating a larger number of Si-H bonds than in the central part of the channel. As a result, during the bias-stress a much larger density of Si dangling bonds can be generated at the gate edges. In addition, water is expected to diffuse quite effectively in the damaged oxide regions, thus enhancing NBTI, as reported for c-Si MOSFETs [5, 7]. In fact, H_2O and related species are likely to depassivate Si-H, through a reaction [7] which yields to positively charged $H3O^+$. As a result of these effects, we can reasonably expect in SA structures an increased interface state and fixed oxide charge generation at the gate edges, thus explaining the observed features.

4. Summary

The effects of hot carriers and self-heating on the electrical stability of p-channel TFTs have been analysed combining experimental data and numerical simulations.

HCE were shown not to appreciably influence the transfer characteristics, while induced a reduction of kink-effect in the output characteristics. These results have been explained by using a self-consistent model based on the trapping of injected hot electrons. Our charge injection model provided a precise evaluation of the extension of the trapped charge regions, at both front and back interfaces. In particular, it has been shown that by decreasing $V_{dstress}$ the injected regions expands from the drain to the source side while the maximum trapped charge density also increases, as injected electrons can access oxide traps located deeper from the oxide/semiconductor interface. By using such trapped charge distributions, it was possible to reproduce the output characteristics variations as well as the minor on-current increase observed in the transfer characteristics after bias stress. Self-heating related instability was found to more seriously affect the device characteristics. From extensive analysis of the phenomenon through numerical simulations, we concluded that the device degradation could be perfectly reproduced by interface state generation and positive charge injection into the gate oxide along the channel and with the presence of additional defects in narrow (100 nm) regions at gate edges. We found that the apparent field effect mobility enhancement, present in SA devices, is a distinctive feature pointing out to the presence of additional defects generated at the gate edges.

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