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Perpendicular Exchange Bias for High Density Magnetoresistance Random Access Memory Application

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The emerging issues of high density integration are inevitable in Magnetoresistive Random Access Memory (MRAM) research field; the bit cell size should be scaled down to the submicron dimension. The conventional MRAM using magnetic tunneling junction device which consists of in-plane magnetization films such as NiFe, Co, and Fe and so on have magnetization curling phenomena when the devices have been patterned into submicron size. Furthermore the magnetization curling will cause the switching field fluctuation, which brings the lower tolerance of writing cross talk by the offset of the magnetoresistance curve. Whereas the perpendicular magnetization films can prohibit the magnetization curling effect at the edge of the patterned elements. We have presented the perpendicular exchange bias of TbFeCo/FePt multilayers with the antiferromagnetic and ferromagnetic layers thickness change for perpendicular MRAM application. The FePt layers have been deposited by in-situ annealing at the 500 ℃ in order to get the L10 structure. The composition of the films were analyzed by the Auger Electron Spectroscopy (AES) and Rutherford Backscattering Spectroscopy (RBS) for the confirmation of AES analysis, the magnetic properties were obtained by Vibrating Sample Magnetometer (VSM). The x-ray diffractometry(CuKα) was employed for the structure identification for 20° ~ 100° 2 theta angle. The (200) peak of the fcc structure is the evidence since it does not overlap with the (111) peak and the appearance of the superlattice reflections (001) and (110) at the angle about 24° and 33°, respectively. The coercivity value shows somewhat change from 120 Oe to 136 Oe according to the FePt thickness. And over the 100 nm FePt thickness, the exchange bias field is reduced drastically. Hence the TbFeCo/FePt multilayer system has to be good correspondence with the conventional exchange anisotropy theory.

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Submicron-Sized MRAM Array with Local Field Switching Architecture

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We have fabricated the Mbit-level MRAM array with local field switching architecture. The front-end process for the driving and peripheral circuit was fabricated by the 0.18 um CMOS technology of DongbuAnam Semiconductor and the back-end process was fabricated by E-beam lithography of NNFC(National Nano Fabrication Center) and photolithography.

The main circuit consists of 8×(16+2*)=144 MTJ cells of 0.3 × 0.4 um^2 size. There are 128 storage cells and 16 reference cells, respectively Additionally, 8 test pattern blocks are included for process monitoring and individual electrical testing for MTJ and transistor.

In this presentation, we will present the performance of array with local field switching architecture and discuss the advantage of those architecture in Mbit level MRAM device.

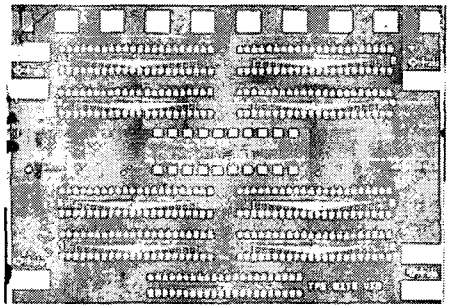

Fig. 1 . Plane view of actual MRAM chip.