Board Level Reliability Evaluation for Package on Package

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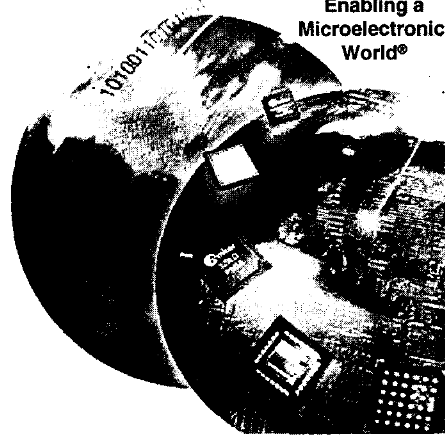
(앰코테크놀로지코리아)

Board Level Reliability Evaluation on PoP



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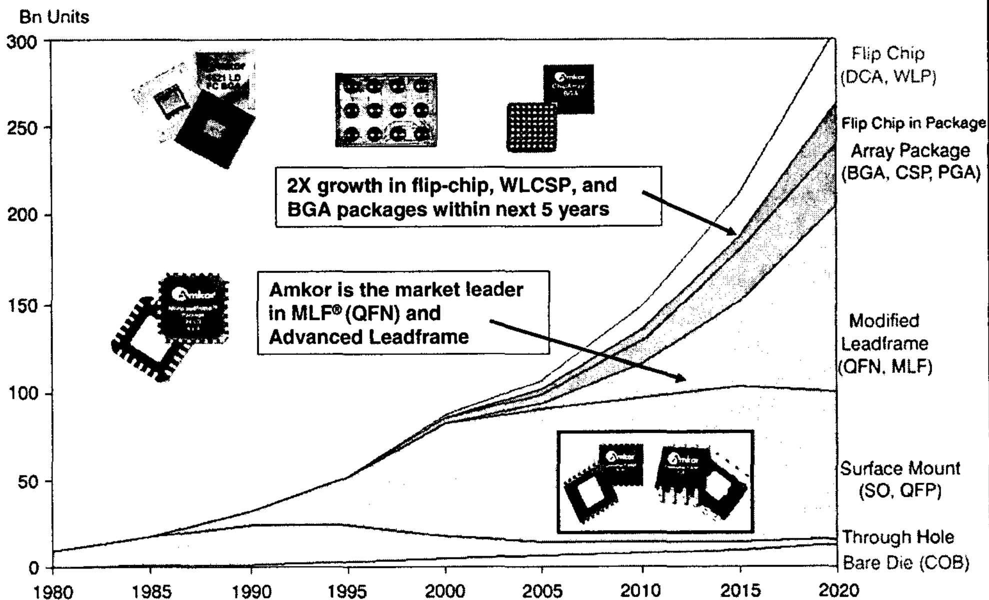
ST H&Q RnD APD2

Advanced Package Growth Forecast



Source: Prismark 2004

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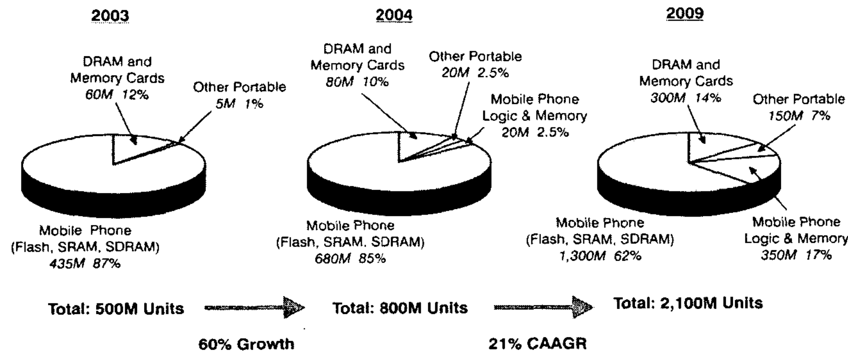
Market Growth in Stacking



Source : *Prismark*

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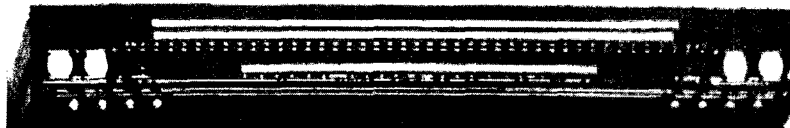
Package on Package (PoP) Introduction



- **Amkor recognized as industry leader in PoP technology**
  - 2 industry awards in 2005
- **PoP technology and infrastructure has been in development at Amkor > four years and production > nine quarters.**
  - PSetCSP was initial work for package stacking applications
    - Joint papers w/ major OEM at 2002 & 2003 ECTC
  - PSvfBGA was developed from 2003, released to production in Q4, 2004
    - 5+ designs in production, 10+ designs under development or qual
    - Many papers/articles in 2005 and 2006
- **Committed to Standardization work for broad industry benefit**
- **PoP applications include:**
  - Mobile phones (base band or applications processor + combo memory)
  - Digital cameras (image processor + memory)
  - Portable gaming (graphics processor + memory)

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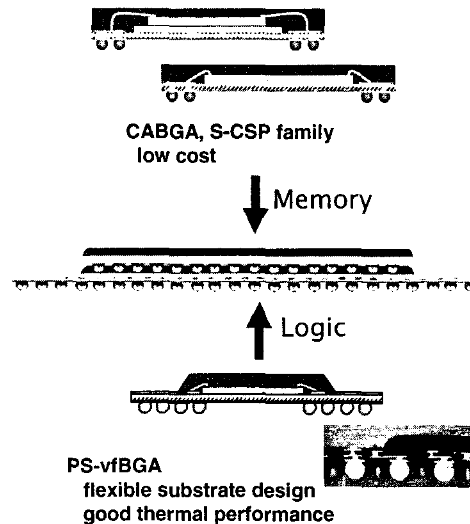
Package Stacking

- **Higher final test yield because each package in stack is tested before final assembly.**
- **Easier to integrate die from multiple suppliers.**
- **OEM *controls supply chain***
  - Stacking during board mount
  - Can dual source memory
  - Easily change memory density
- **Ideal for logic plus memory integration.**



Stacked Die vs. PoP – Trade offs

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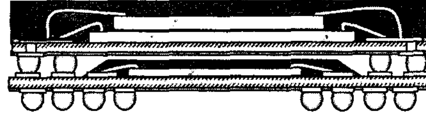
Stacked Die	PoP
Prospects • IDM ownership • Smaller body size and lower package profile (typ: 1mm / side and 0.2m height) • Standard SMT assembly • *Broad infrastructure*	*Prospects* • OEM Ownership • Flexible sourcing: (separate logic vs. memory sources, broader memory combo options, facilitate memory capacity increases late in platform schedule • Tested at individual package level for Known Good Device
Concerns • KGD required for high product yield • Single-sourced product for logic + memory (limited combinations available) • New development needed to change a device or handle die shrink • Sourcing, compound yield and multi test: - Can lead to higher total cost	*Concerns* • Slightly larger / thicker Package stack • Status of emerging JEDEC standards • Coordinate design for bottom and top packages - Electrical and BLR validation • *Infrastructure for package stacking*

Reliability Issues on PoP

- **Structural effects on BLR**
  - Die size
  - Pad & solder mask size
  - Solder ball size & height
  - Substrate thickness
- **Material effects on BLR**
  - Solder alloy
  - Pad finish
  - Underfill material
  - Other BOM
- **Process effects on BLR**
  - Stacking process
  - Reflow temperature
- **Test type**
  - Temperature cycling test
  - Drop test



Package on Package
(PS*vf*BGA + *stacked* CSP)

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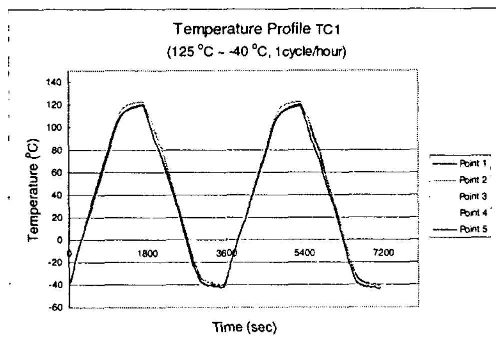
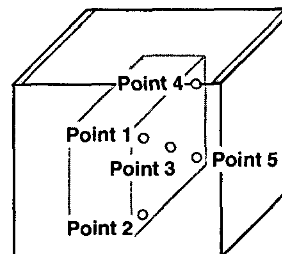
Board Level Temperature Cycling Test

- **Test condition (JEDEC JESD22-A104)**
  - -40 ~ 125'C, 1cycle/hr
  - Slow ramp rate, 18min ramp, and 12min dwell
  - Continuous in-situ electrical monitoring



Temperature profile that was used for testing 5 point measurement



Temperature measuring points in chamber

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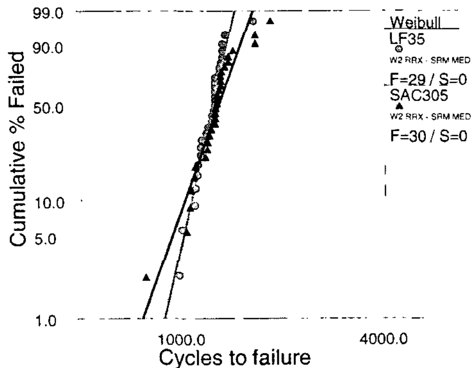
Board Level Temperature Cycling Test

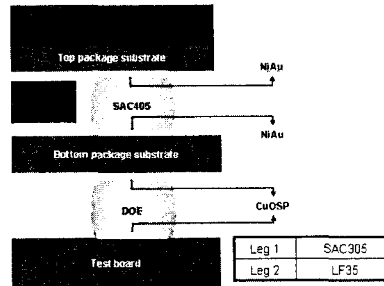
- **Material effects : solder alloy**



$\beta 1=12.66, \eta 1=1269.27, \rho=0.95$
$\beta 2=8.06, \eta 2=1341.89, \rho=0.94$

For NiAu / OSP pad finish, SAC305 ~ LF35

- **Top package**
  - **14 x 14mm, 152 I/O, 0.65mm pitch**
  - **SAC405 solder alloy**
  - **NiAu pad finish**
- **Bottom package**
  - **14 x 14mm, 353 I/O, 0.5mm pitch**
  - **NiAu / CuOSP pad finish**



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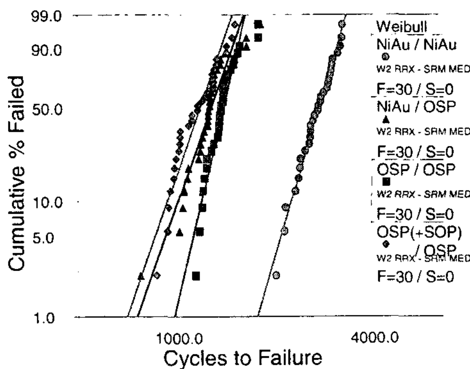
Board Level Temperature Cycling Test

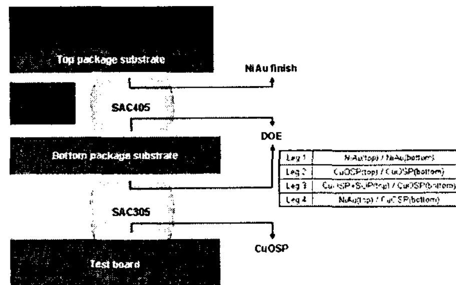
- **Material effects : metal pad finish**



$\beta 1=9.64, \eta 1=2860.25, \rho=0.99$ $\beta 3=12.03, \eta 3=1445.49, \rho=0.93$
$\beta 2=8.06, \eta 2=1341.89, \rho=0.94$ $\beta 4=8.14, \eta 4=1241.15, \rho=0.96$

For SAC305,
NiAu / NiAu >> OSP / OSP > NiAu / OSP,
OSP(+SOP) / OSP

- **Top package**
  - **14 x 14mm, 152 I/O, 0.65mm pitch**
  - **SAC405 solder alloy**
  - **NiAu pad finish**
- **Bottom package**
  - **14 x 14mm, 353 I/O, 0.5mm pitch**
  - **SAC305 solder alloy**



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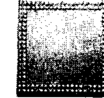
Board Level Temperature Cycling Test

- **Material effects : 2nd level underfill material**
  - Top package
    - 14 x 14mm, 152 I/O, 0.65mm pitch
    - SAC305 solder alloy
    - NiAu pad finish
  - Bottom package
    - 14 x 14mm, 353 I/O, 0.5mm pitch
    - NiAu / NiAu pad finish
    - SAC305 solder alloy

vfBGA



stacked CSP

Underfill name		No underfill	Underfill A	Underfill B	Underfill C	Underfill D	Underfill E	Underfill F	Underfill G
Type		N/A	[illegible]	[illegible]			[illegible]	[illegible]	[illegible]
Dispensing pattern			Full	Full	Full	Full	Full	Full	Full
Viscosity (poise)			40	20	100	20	220	2500cps	
Filler size (ave/max) [um]			0	0	5/24	2/10	2/10		
Filler content			0%	0%	70%	65%	50%	0%	0%
Tg (DMA)	(℃)				140	162	90	119	
Tg (TMA)	(℃)		66.97	62.88	113 05	50 29	60.14	89	94 36
CTE (α1)	(ppm/℃)		61 5	69 4	19 9	51 9	42.8	58	59
CTE (α2)	(ppm/℃)		129	195	83	181	125	193	195
F. strength	MPa		N/A	69 8	150	108	-	-	-
F. modulus @-25℃	GPa		3 25	2 63	8.39	1.7	1 57	3.21	2.35
F. modulus @25℃			3 08	1 92	8	1.63	1 51	2.9	2.02
F. modulus @125℃	MPa		16 4	13 3	5098	1.45	1.82	18.6 ·	27.6
F. modulus @220℃			14 2	18.1	5 11	2.71	2.95	21.5	17.4
F. modulus @245℃			15 7	20 9	508	3.62	3.79	27.6	27.6
F. modulus @260℃			19 2	22.5	504	4.33	4.51	35.1	36

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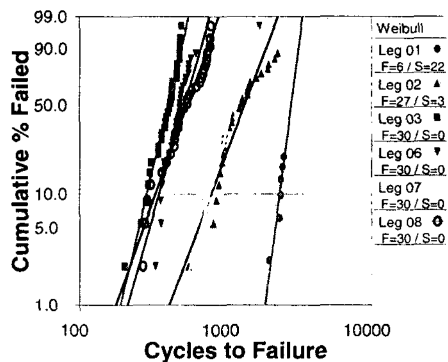
Board Level Temperature Cycling Test

- **Material effects : 2nd level underfill material**



$\beta1=10.410, \eta1=2882.4, \rho=0.942$ $\beta4=4.754, \eta4=560.0, \rho=0.813$
$\beta2=3.584, \eta2=1481.8, \rho=0.942$ $\beta5=5.017, \eta5=1209.8, \rho=0.920$
$\beta3=5.669, \eta3=426.5, \rho=0.987$ $\beta6=3.773, \eta6=597.5, \rho=0.981$

As of TC -40~125'C x500 cycle

Leg NBR	U/F Name	Dispensing Pattern	Filler Content	Results	Remarks	1st Failure
1	No underfill	N/A	N/A	PASS	1 failure from SMT error	182 *
2	Underfill A	Full	None	PASS	No failure	
3	Underfill B	Full	None	FAIL	4 of 30 failures in BO net 24 of 30 failures in TC net 30 of 30 failures in TM net	202
4	Underfill C	Full	70%	PASS	No failure	
5	Underfill D	Full	65%	PASS	1 of 30 failure in TM net	402 *
6	Underfill E	Full	50%	FAIL	19 of 30 failures in TM net	329
7	Underfill F	Full	None	PASS	No failure	
8	Underfill G	Full	None	FAIL	1 of 30 failure in BO net 1 of 30 failure in TC net 12 of 30 failure in TM net	270

<u>As of x2500 cycles,</u>

Leg NBR	U/F Name	NBR of failure	1st Failure	Mean life	Char. life (η)	Slope (β)
1	No underfill	6/27	1968	2746.8	2882 4	10.410
2	Underfill A	27/30	555	1335.0	1481 8	3.584
3	Underfill B	30/30	202	394.4	426.5	5.669
4	Underfill C	0/30	N/A	N/A	N/A	N/A
5	Underfill D	4/30	1791	N/A	N/A	N/A
6	Underfill E	30/30	329	512.7	560 0	4.754
7	Underfill F	30/30	681	1111.0	1209.8	5.017
8	Underfill G	30/30	270	539.8	597.5	3.773

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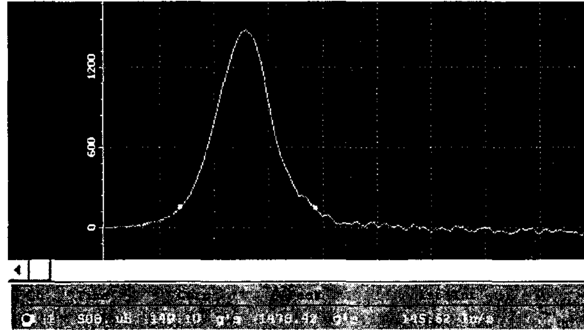
Board Level Drop Test

- **Test condition (JEDEC JESD22-B111)**
  - 1500 Gs, 0.5msec duration, half sine pulse
  - 200~400 drops were conducted
  - The electrical resistance of each net was measured in-situ during each drop
  - Rebound is not allowed



Drop pulse shape for JEDEC drop condition

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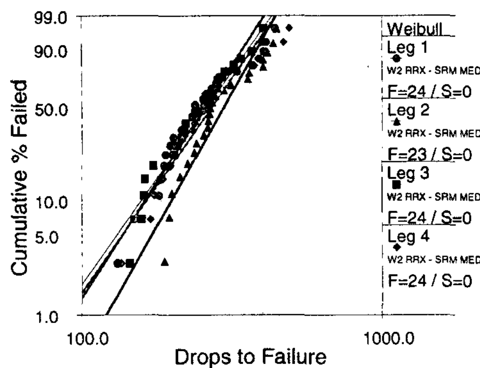
Board Level Drop Test

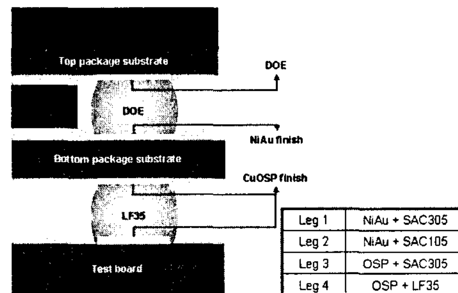
- **Material effects : solder alloy & metal pad finish**



$\beta1=3.78, \eta1=286.21, \rho=0.96$ $\beta3=4.13, \eta3=279.59, \rho=0.97$
$\beta2=4.71, \eta2=319.77, \rho=0.95$ $\beta4=3.81, \eta4=296.11, \rho=0.95$

NiAu + SAC105 is best,
For NiAu pad finish, SAC105 > SAC305
For CuOSP pad finish, LF35 > SAC305

- **Top package**
  - **12 x 12mm, 128 I/O, 0.65mm pitch**
- **Bottom package**
  - **12 x 12mm, 305 I/O, 0.5mm pitch**
  - **LF35 solder alloy**
  - **NiAu / CuOSP pad finish**



Leg 1	NiAu + SAC305
Leg 2	NiAu + SAC105
Leg 3	OSP + SAC305
Leg 4	OSP + LF35

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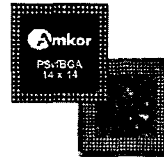
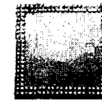
Board Level Drop Test

- **Material effects : 2nd level underfill material**
  - **Top package**
    - **14 x 14mm, 152 I/O, 0.65mm pitch**
    - **SAC305 solder alloy**
    - **NiAu pad finish**
  - **Bottom package**
    - **14 x 14mm, 353 I/O, 0.5mm pitch**
    - **NiAu / NiAu pad finish**
    - **SAC305 solder alloy**



vfBGA



***stacked* CSP**

Underfill name		No underfill	Underfill A		Underfill C	Underfill D		Underfill F	
Type		N/A	[illegible]					[illegible]	
Dispensing pattern			Full		Full	Full		Full	
Viscosity (poise)			40		100	20		2500cps	
Filler size (ave/max) [um]			0		5/24	2/10			
Filler content			0%		70%	65%		0%	
Tg (DMA)	(℃)				140	162		119	
Tg (TMA)	(℃)		66 97		113 05	50 29		89	
CTE (α1)	(ppm/℃)		61 5		19.9	51.9		58	
CTE (α2)	(ppm/℃)		129		83	181		193	
F. strength	MPa		N/A		150	108		-	
F. modulus @-25℃	GPa		3.25		8 39	1 7		3 21	
F. modulus @25℃			3 08		8	1 63		2 9	
F. modulus @125℃	MPa		16 4		5098	1 45		18 6	
F. modulus @220℃			14 2		5 11	2 71		21 5	
F. modulus @245℃			15 7		508	3 62		27 6	
F. modulus @260℃			19 2		504	4 33		35 1	

Board Level Drop Test

- **Material effects : 2nd level underfill material**
  - As of 400 drops,

Leg NBR	U/F Name	Dispensing Pattern	Filler Content	Total NBR of drops	NBR of failures	Mean life	Failure modes
11	No underfill	N/A	N/A	400	24/24	137.8	Bottom PKG : PCB pad / IMC
12	Underfill A	Full	None	400	3/24		Bottom PKG : PWB trace crack
13	Underfill C	Full	70%	400	0/24		No failure
14	Underfill D	Full	65%	400	12/24	660 9 *	Bottom PKG : PCB pad / IMC
15	Underfill F	Full	None	400	0/24		No failure

* Data was extrapolated from the test results

- Underfill C & F have no failure until 400 drops
- Underfill A has 3 failures until 400 drops but these failure are confirmed as test board trace crack not solder joint failure

Summary

Factor		Board level TC test	Board level Drop test
Structure	Metal pad & SMO size	- Large SMO size is better	- Large SMO size is better
	Substrate thickness	- Thick substrate is better	- Substrate thickness is not a significant factor for drop test
Material	Solder alloy	**- Not so big differences over Pb-free solder and NiAu, OSP finish**	**- Ni/Au + SAC105, CuOSP + LF35** are better
	Pad finish	**- NiAu / NiAu is best**	**- CuOSP is best**
	Underfill	**- Several underfills (reworkable) are passed TCG x500 cycles**	**- Underfill lots have better performance than non-underfill lots**
Process	Multiple reflow	- Multiple reflow is not a significant factor for TC test	N/A
	Peak temp.	- Higher peak temperature is worse than STD	N/A
	Stack method	- No big difference between pre-stack and SMT stack	- Flux dipping is better than paste dipping but failure rate is more faster

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