차세대 기판 공정 기술동향

강 남 기 센터장
(KETI)

차세대 SoP-L 기판 공정 기술 동향

2007. 4.4

전자소재패키징 연구센터

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KE-TI 전자부품연구원

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Contents

1. Introduction of SoP-L
2. Fine Patterning Technology
3. Embedded Passive & Active Device

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Introduction of SoP-L

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System on Package 기술분류

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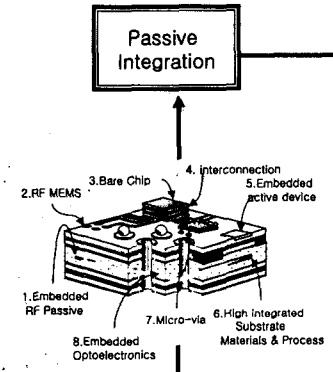

Passive Embedded SOP-L
- Cost effective Solution
- Effective @ f < 5GHz

유기소재기반 (Laminated) SOP-L

Passive Embedded SOP-C
- Performance effective solution
- Effective @ 2< f < 50GHz

세라믹 기반 (Ceramic) SOP-C

Passive Embedded SOP-D
- Size effective solution
- Effective @ f > 20GHz

박막 기반 (Deposited) SOP-D

MCP (Multi Chip Package)
- Active Integration Solution

Chip Stacking (Deep etch, Wafer thinning)

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SoP-L 핵심 기술

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System On Package (SOP)-L (Laminate) 기술

✓ Organic기판 (주로 PCB)내에 집적화하는 기술
- 회로 집적화, 부품 집적화 etc

부품의 복합화 추세

(Integrated Passive Devices)

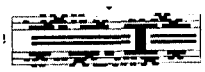
단순 칩 부품

어레이 칩 부품

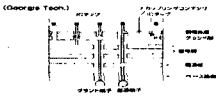
수동 소자 내장모듈

기판에서 부품내장화 방향

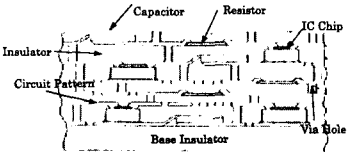
(Integral Substrates)



Build-up 다층기판



수동소자 내장형 다층기판



수동·능동 소자
내장형 모듈/기판

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SoP-L 기술 개발 필요성

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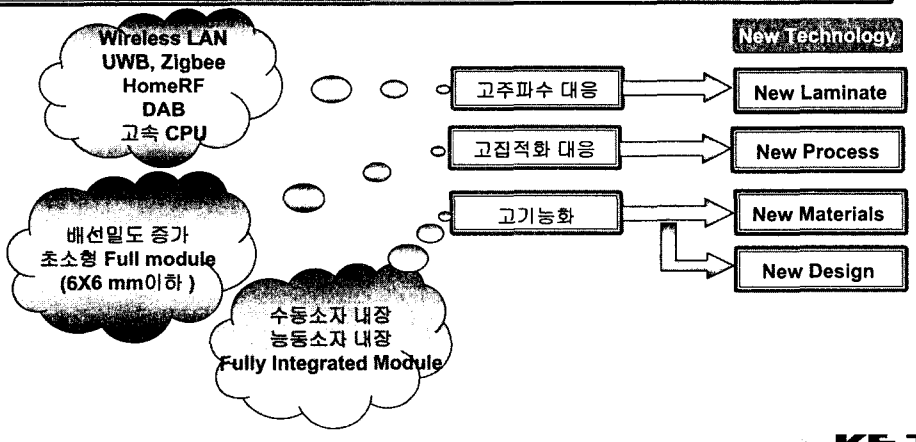
차세대 회로 구현기술

- 저가의 범용 부품기술인 PCB 기술에 차세대 신기술 접목 필요성 증대
- 디지털 회로 → RF + Digital(B.B.) 를 일체화하기 위한 기술로 진화

➡ 고주파수, 저전력, 광대역화 를 통해 대용량 정보전송을 위한 회로 구현
SOP -L 공정 및 설계에 대한 기술 개발이 시급함.



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SoP-L 시장 동향

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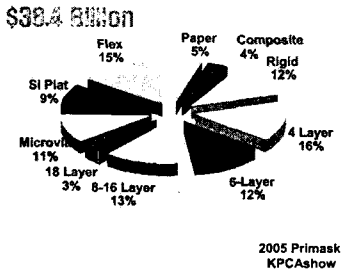
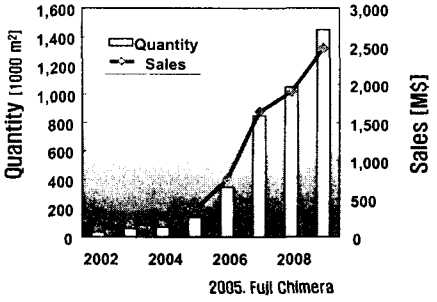
◆ PCB 관련 시장은 2004년 38.4 Billion $ 에서 2009년 52.3 Billion $로 성장할 것이 예측됨.
이중 SOP 관련 시장은 microvia, multi-layer, Flex. 분야로 70% 정도를 차지함 (2004년기준).
◆ EPD 관련 분야는 2007년 현재 15 억불의 정도의 시장이 형성되었으며,
2010년 까지 연평균 170%의 성장이 예상됨.
➡ 디지털 컨버전스에 따른 차세대 전자기기의 출현으로 급속한 성장이 예상되는 분야임.

■ 2004년 PCB market 분석



2005 Primask
KPCAshow

■ Embedded PCB Market Prediction



2005. Fuji Chimera

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SoP-L 기술 TREND

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		'05	'06	'07	'08	~'10
Application	단말기	PDA, DMB Phone	Smart Phone			
	Main Chip	MSM : SoC[1] Memory : Chip Stack RF : Module化		Chip 융합 SoC + Memory +수동소자		SoP SoC/MCP/수동소자 Sensor & Filter
	Pitch	0.5/0.4mm	0.3mm	0.2mm		
	Passive Comp	0.5CSP 0603	0.4CSP 0402	Embedded Passive+0402		Thin Core PKG
	❑ Rigid	Conventional Build-up STG	Filled Via	Filled stack Via + Embedded passive		•Embedded passive •OPTICAL PCB
		Stack-via Filled via 1stack	2stack ALL IVH			
	❑ Rigid-Flex	SBL/STG 6 - 4 - 6	STG/Filled Via 8-4-8 8-2-8	Filled via + Stack via 8-4-8(ALL IVH)		
	❑ Fine Pattern	50/50㎛	35/35 ㎛	25/25 ㎛	15/15 ㎛	10/10 ㎛
	❑ Micro Via					
	-Laser via	80㎛	50㎛	30㎛	20㎛	10㎛
	-Paste filled via	100㎛	100㎛	80㎛	80㎛	60㎛
	❑ Solder Mask clearance	50㎛	40㎛	20㎛	15㎛	10㎛

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Fine Patterning Technology

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PCB Pattern Road Map

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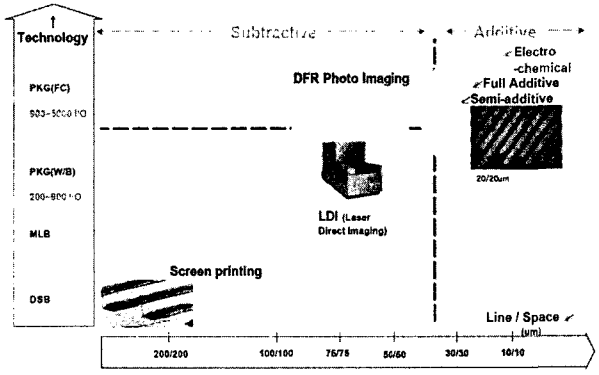
Fine Line Circuit Formation



- 회로 Pattern 이 미세화되면서 기존의 Screen Printing → Lithography, Etching → Additive 방법으로의 전환이 진행되고 있음.

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Wet Etching Technology

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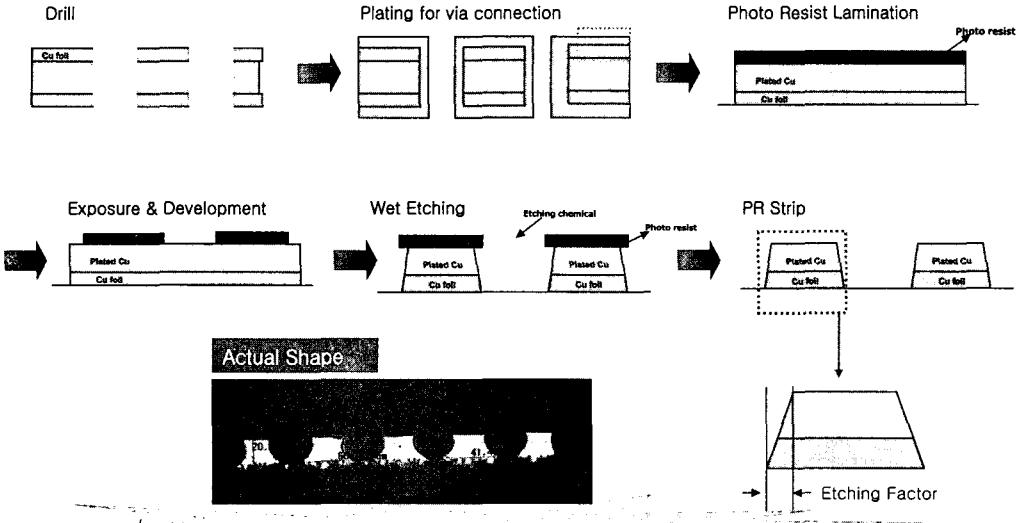
✓Conventional Subtractive Process



√ Very Difficult to get fine Line under 30 micron due to Etching factor

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Semi additive patterning

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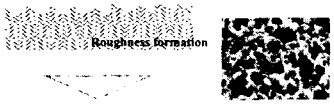
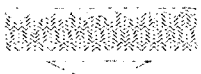
○ Fine Line Circuit Formation of PCB

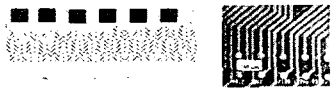
Surface Treatment



Seed Layer formation

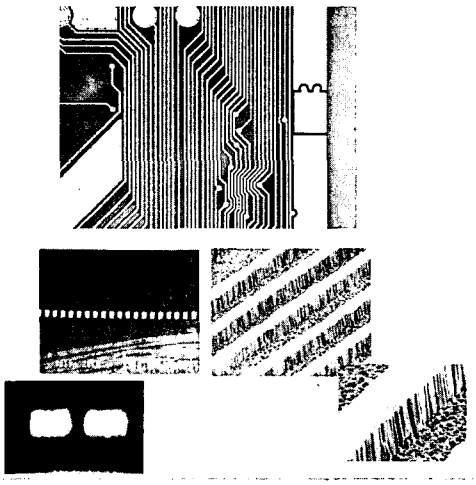


PR patterning & plating



PR & Seed Layer removal

✓ 25/25㎛ Pattern Images



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Thick-Film Photolithography

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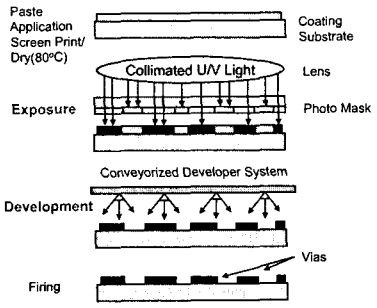
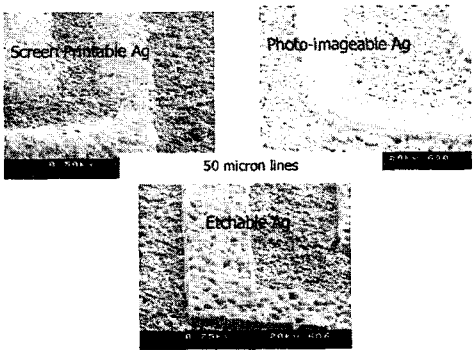
Thick-Film Photolithography : Advantages





- ✓ Higher line & space resolution
- ✓ More precise line definition
- ✓ Lower cost process than thin film
- ✓ Photoimgeable process
- ✓ Photoetchable process

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LDI (Laser Direct Imaging)

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✓ **Subtractive 방법과 Additive pattern법의 중간 단계**

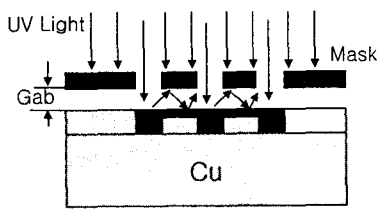
LDI Systems Exhibited at 2005 JPCA Show

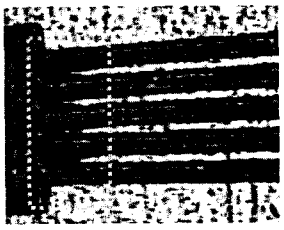
LDI Makers	Model	Wave(nm)	Min L/S(um) *	Max Panel(mm)
Orbotech	Paragon-8000	355	25-50	635×812
Pentax	DI-Series	405	15-35	530×630
Hitachi Via	DE-Series	405	10-40	550×650
Fuji Film	INPREX	350-410	15-25	530×640
Dainippon Screen	Mercurex	350-420	20±2	540×640

* Minimum L/S capability depends on the models

(2005 JPCA, Company brochure)

✓ **Why LDI ?**





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LDI (Laser Direct Imaging)

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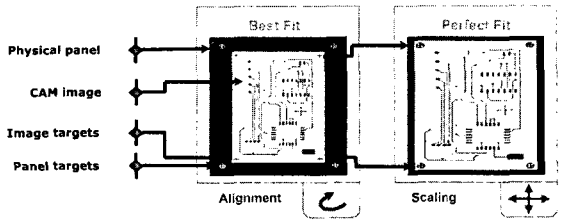
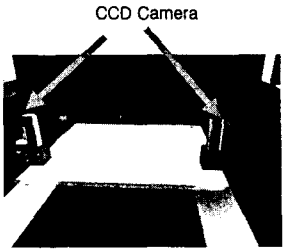
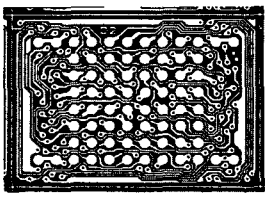
✓ Don't need Pattern Mask!



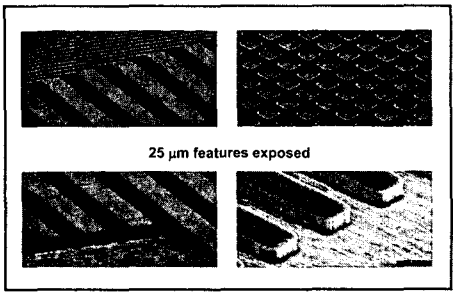


✓ LDI alignment: Pattern



CSP
Outer layer imaging by LDI

Sequential Build-up
Conformal mask imaging by LDI,
25 μm annular ring



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LDS (Laser Direct Structuring)

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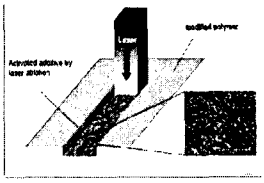
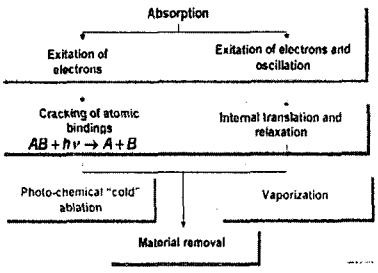
Mechanism of LDS

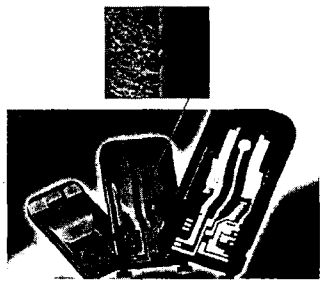
Injection Molding → Laser Structuring → Metallization(plating)

-LDS compatible plastics material : doped with a metal organic compound

- Laser Activation : physicochemical reaction through induced laser energy that breaks the organic compound and expose the metal atoms for the metallization







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LDS (Laser Direct Structuring)

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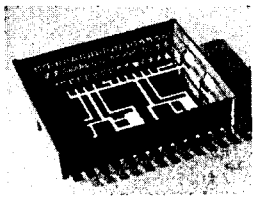
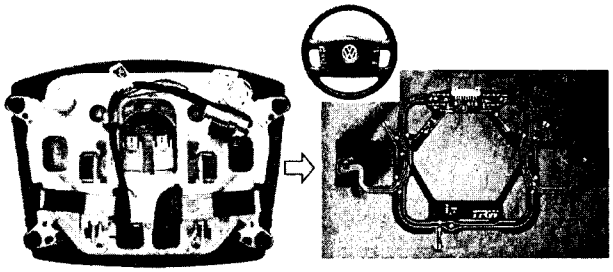
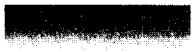
Applications



Solid State Power Controller Case

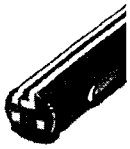


Multifunctional Steering Wheel



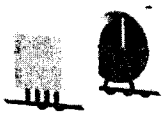
Hearing Aids

Electrostatic micro valves



Rotary Encoder Casing

Position Sensor



Capacitive Inclination Sensors

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Inkjet Technology

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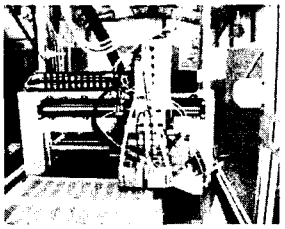
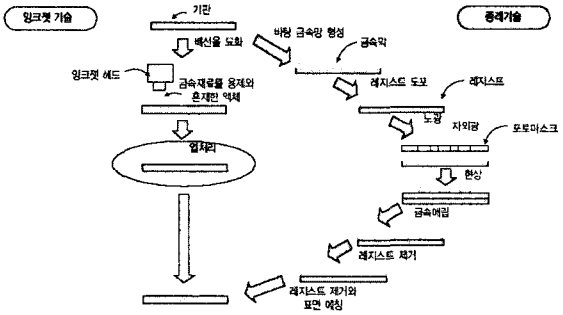
PCB Using Inkjet Technology





- 필요한 재료를 원하는 위치에 도포함으로써 재료의 소비를 최소화
- DOD 방식의 디지털 제어 → 분사량 정밀 조절, 고해상도 용이
- 노광/에칭공정 단계 불요 → 폐수의 양 저감(친환경 공정기술)
- 공정 단계의 축소에 따른 공정비용의 획기적 절감

** Source: 월간 SMT PCB Korea, 2006년 2월호*

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Inkjet Technology

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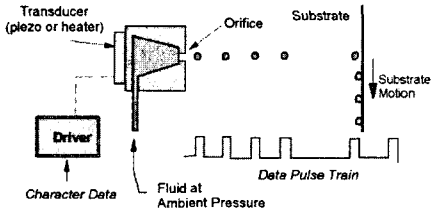
Ink-Jet Technology : DoD & Examples

Demand Ink-Jet Technology



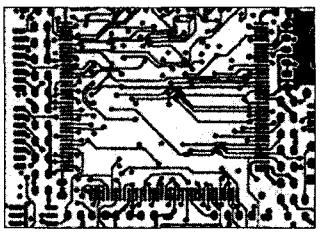


그림 6. PR를 잉크젯 프린팅한 사례

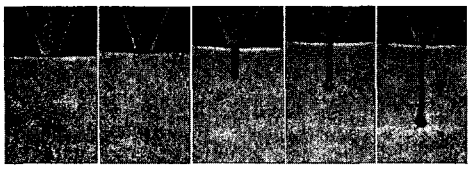


Figure 1 Demand mode ink-jet glass device generating 50μm diameter drops at 2kHz

Figure 6 Ink jet printed embedded resistor using conductive polymer; *100 ohm/sq.*

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Aerosol Deposition

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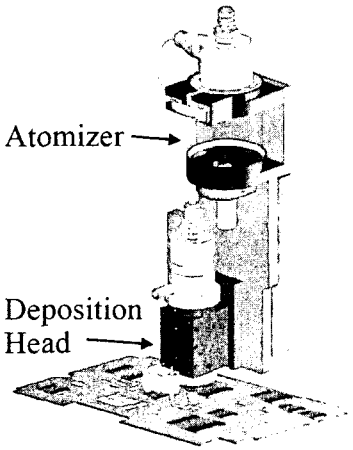
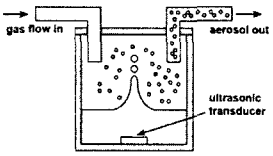
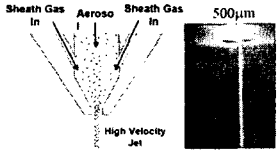
What is Aerosol Deposition ?



✓**Ultrasonic Atomizer**



✓**Aerosol Jetting**



- **Precise Deposition, Aerosol Drops**
- **Mask less, efficient Material Usage**
- **Mesoscale (10-100 μm), Conformal**
- **Laser Treatment Option for Low-Temperature Substrates**
- **Wide Range of Materials Compatibility**
- **Wide Range of Prototyping and Manufacturing Applications**

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Aerosol Deposition

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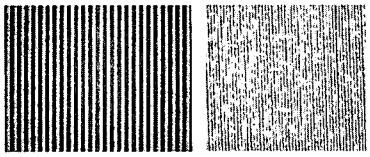
타 기술과의 비교

	Inkjet	Aerosol Deposition	Screen Print	Thick Film Photolithography
Feature Size	~ 50 um	10 um	~ 100 um	40 um
Droplet Size	20-50 um	1-5 um	N/A	N/A
Standoff Height	< 1 mm	> 5 mm	Contact	Contact
Metal Contents in Inks	Low	Medium	High	High
Viscosity	6-8 cP	0.7-1000cP	100kcP	100kcP
Deposition Rate	0.1 mm^3/s	0.25 mm^3/s		

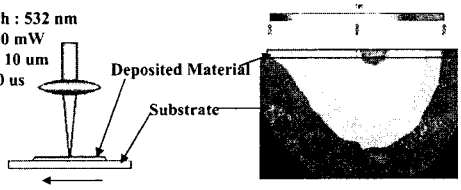


5 um line/space　　2 um line/space

Pd on Sapphire

v **Laser Treatment for Low Temperature Substrates**

Wavelength : 532 nm
Power : 100 mW
Spot Size : 10 um
Dwell : 100 us



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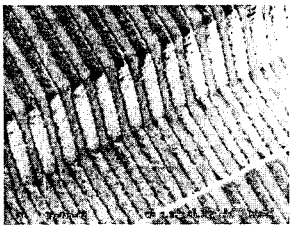
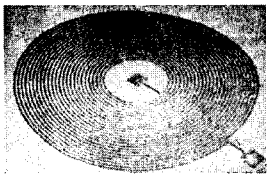
Aerosol Deposition

22

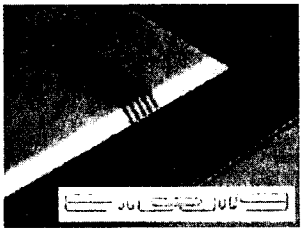
Applications



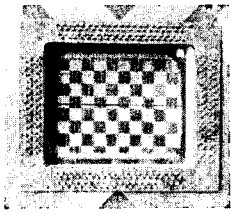
Conformal Deposition
50 um lines into 500 um trench

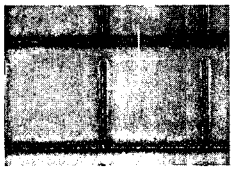


Low Temp. Flexible Substrate
(Ag on Kapton)



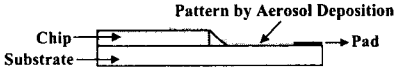
Chip on Board (RF-ID)

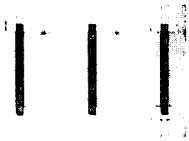




Polymer TFT Display
Ag on PMMA, Resistivity ~ 8 μohm-cm

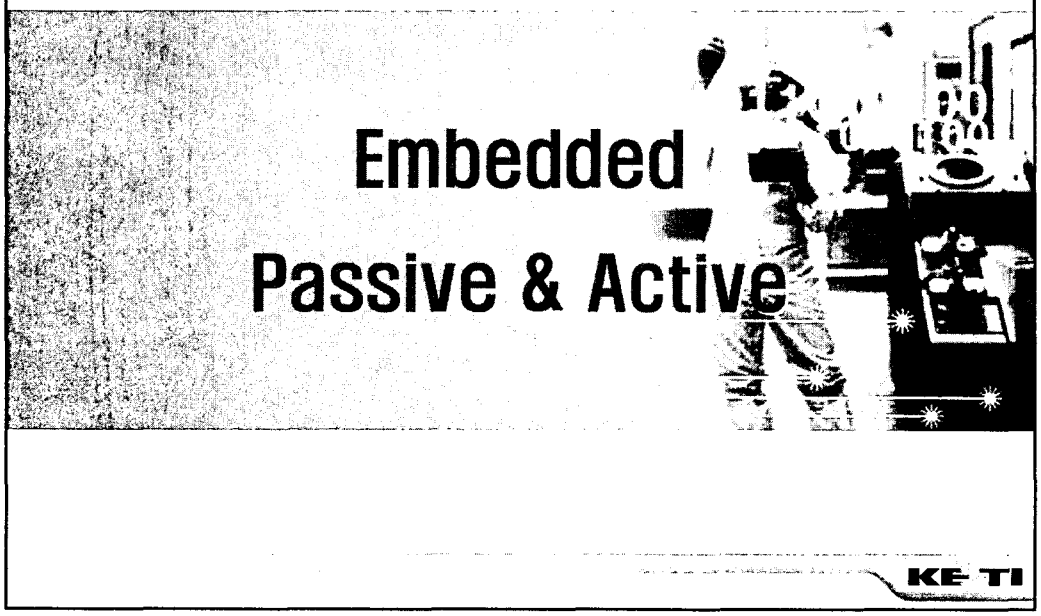
Pattern by Aerosol Deposition

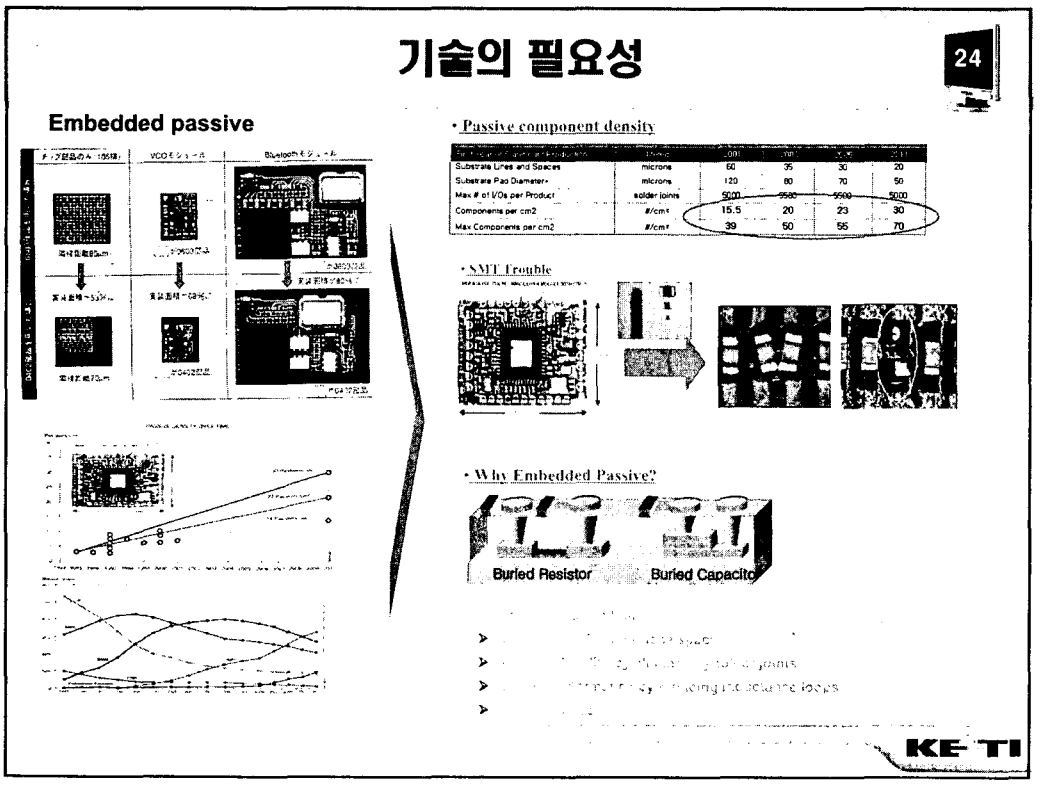




Embedded Passives
Carbon Resitors on FR-4

KE-TI


Embedded
Passive & Active
KE-TI


기술의 필요성
24
Embedded passive
• Passive component density
Substrate Lines and Spaces
microns
60
35
30
20
Substrate Pad Diameter
microns
120
80
70
50
Max # of I/Os per Product
solder joints
5000
5500
5500
5000
Components per cm2
#/cm²
15.5
20
23
30
Max Components per cm2
#/cm²
39
50
55
70
• SMT Trouble
• Why Embedded Passive?
Buried Resistor
Buried Capacito
KE-TI

Trends of Embedded discrete chip

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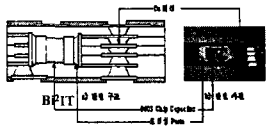
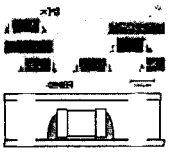
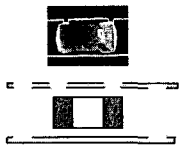
	구조1 DT써키트,덴소	구조2 아쯔시다	구조3 KETI
형성 방법			
비고	•Cavity 공정후 부품 삽입 • 전도성 Paste 또는 도금으로 전극연결 •인쇄 공정 필요 •라미네이트 공정후 추가 via가공 필요	•SMD공정으로 부품실장 – soldering 공정필요 •SMD공정 후 적층과 via가공으로 connection •적층라미네이트 공정시 솔더 joint 부분 파괴우려 •솔더링 두께 만큼 두께증가	•Cavity 공정후 부품 삽입 •부품전극부위에 via가공과 도금으로 connection •공정이 간단하고 Soldering 필요 없음 •구조 1,2에 비해 두께가 가장 낮음.

KE-TI

Embedded Resistor technical Trend

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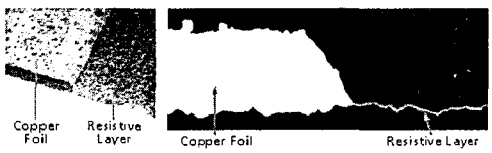
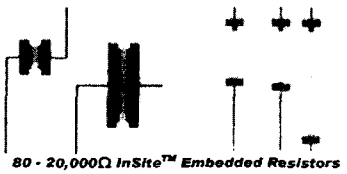
제 조 공 정	후 막 법 (인쇄)		박 막 법		Ink Jet
	저온 경화형	고온 소성형	박막 에칭 (박판접합)	도 금	
면 저 항 (Ohm/sq.)	1 ~ 1 M	10 ~ 10 K	25 ~250 1000	25 ~100	100 600
Competitors	Asahi	Dupont	Gould, OmegaTech, Shipley	McDermid	MicroFab Cabot
Tolerance	±10 ~ ±20%	±5 ~ ±10%	±15%	±10~15%	±2% (?)
장 점	넓은 저항 범위 양산화 용이	고 신뢰성	널리 사용 중 Trimming 용이	Trimming 용이	공정이 단순함 박막화 가능
단 점	구리 배선의 부식, 장시간 Trimming	고온소성 등 공정 복잡, 양산화 불리	저항 구현 범위 협소, 환경문제	저항 구현 범위 협소, 환경문제	연구단계



TCR of Gould



InSite of Rohm & Haas / Shipley

KE-TI

Thin Film Etching

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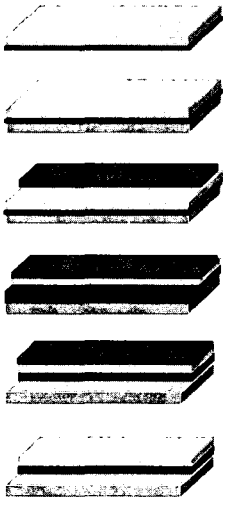

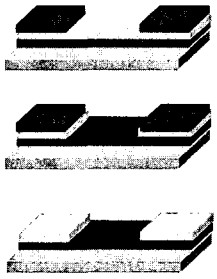

Supplier	Product	Material
Ohmega Technologies, Inc.	Ohmega-Ply®	NiP
Gould Electronics	TCR®	NiCr & NiCrAlSi
Shipley	InSite™	doped Pt

Material thickness (µm)	0.04...0.4
Rs (ohms/sq)	10...1k
Untrimmed tolerance (%)	±5...±10
TCR (ppm/°C)	-80...-110
Max power dissipation (W/cm2)	12...80
Change in thermal cycling (±%)	-0.08...-4.2

KE TI

Plating

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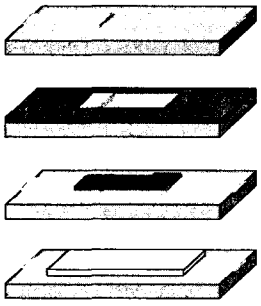
M-Pass of MacDermid



Some basic properties of M-PASS™ embedded resistors

Material thickness (µm)	0.05...0.20...
Rs (ohms/sq)	25...100
Untrimmed tolerance (%)	±10...±20
TCR (ppm/°C)	<100
Max power dissipation (W/cm2)	31
Change in thermal cycling (±%)	<1

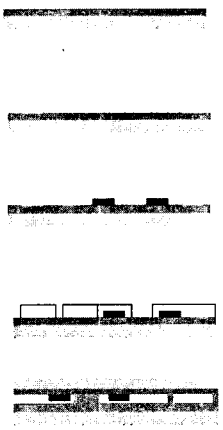
→ 에칭형보다 공정이 단순하지만 **lower sheet resistance**

KE TI

Ceramic Thick Film

29

Interra of DuPont



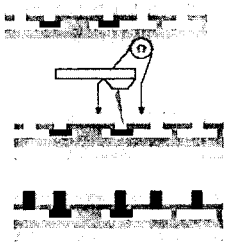
Adhesion promoter is printed on a copper foil. paste is dried and fired

X-ray fiducials are printed and dried

Resistor pastes are printed and dried; all pastes are fired

Laser trim encapsulant is printed, dried and cured

Foil is laminated to form an innerlayer core



Standard innerlayer process is performed to reveal the resistors

Resistors are trimmed

Encapsulant paste is printed, dried and cured

Some basic properties of ceramic thick film embedded resistors

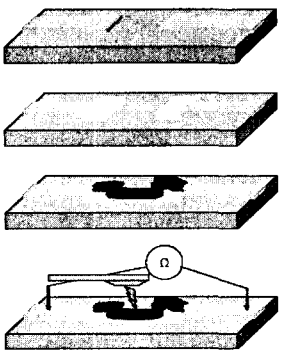
Material thickness (μm)	~25
Rs (ohms/sq)	10...10k
Untrimmed tolerance (%)	±10...±25
TCR (ppm/°C)	-170...140
Max power dissipation (W/cm2)	6.5...92.5
Change in thermal cycling (±%)	0.5...1

KE-TI

Polymeric Carbon Paste

30

TU-XX-08 of Asahi Chemical Research Lab.



Standard innerlayer process is performed to form the circuitry

Terminal pad material is applied either by plating or by screen printing

Resistor paste is screen printed and cured

Resistors are laser trimmed

Some basic properties of PTF embedded resistors

Material thickness (μm)	10...25
Rs (ohms/sq)	10...100k...10M
Untrimmed tolerance (%)	±10...±30
TCR (ppm/°C)	±200...±700
Max power dissipation (W/cm2)	1.5...6.5
Change in heating test (±%)	2...5

→ 넓은 범위의 저항체 구현이 가능하지만 **tolerance** 및 신뢰성이 약점

KE-TI

Photo-patterned PTFR

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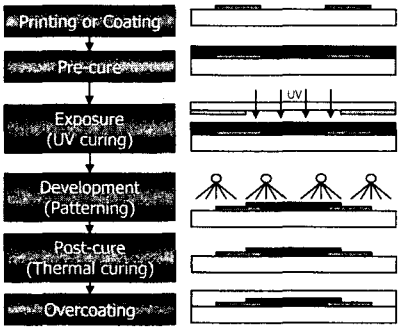
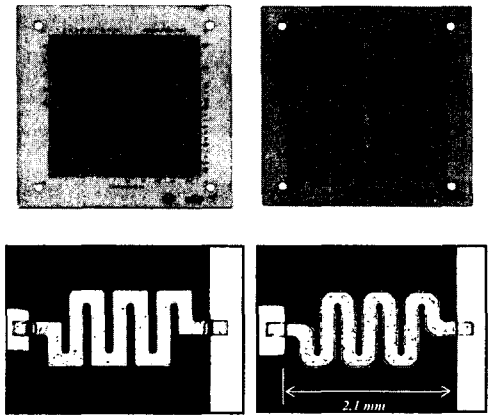
Under development in KETI





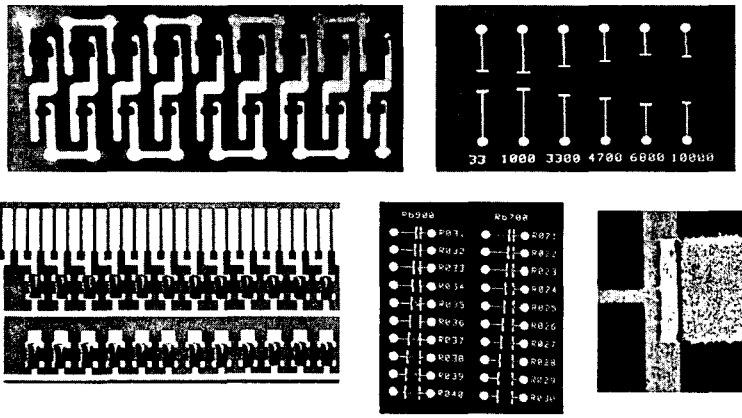
→ 작은 면적에 고저항체 구현이 가능

→ 아직은 **tolerance** 및 신뢰성 약점, **1K** 이하 저항체를 구현하기 쉽지 않음

KETI

Ink Jet Printing

32



→ **Low cost, environment-friendly, simple process**

→ **Problems: Low resistance, limited ink material**

KETI

Flexible Buried Resistor

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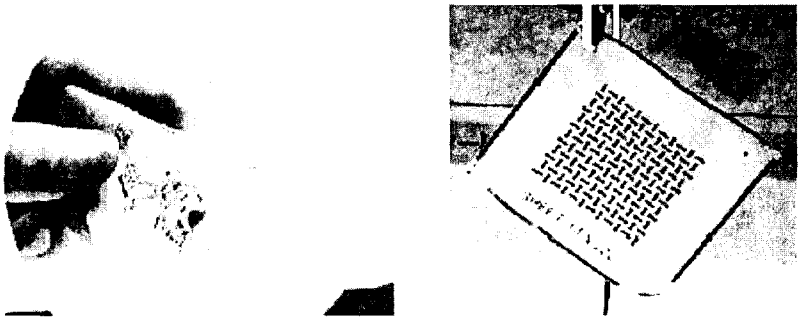

→ **R, C, L in flexible substrate materials**

→ **Buried R in LCP or flexible sub.**

KE TI

Materials for Embedded Capacitor

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Commercial Materials

Maker	Sanmina	Gould	Oak-Mitsui	DuPont	3M	Gould	Matsushita	Huntsman (Vantico) W/ Motorola	Asahi	DuPont
Trade Mark	ZBC2000	TCC	Fara-Flex	Interra	Epoxy	TPL	R5747	Problec (Mezzanine)	CX-16	Interra
Materials	FR-4	Polyimide	Epoxy	Filled Polyimide	$BaTiO_3$ Epoxy	$BaTiO_3$ Epoxy	Inorganic filler	$BaTiO_3$ Photosensitive Epoxy	$BaTiO_3$ Epoxy	Sintered $BaTiO_3$
Dielectric constant	4	4	4	4~15	16	24.3	16	26~30	40~50	1500
Thickness (um)	25, 50	25, 50	10, 25	8~25	8~20	4~25	50	12~50	12~40	10~20
Capacitance (nF/in^2)	0.5~0.9	0.5~0.9	1~2	0.9~11	Max.10	5.4	1.8	10	5~20	300+

- 40% of total passive components
- Important roles in electric circuit

Cf. ECURL of Daeduck

KE TI

Commercial_ Motorola

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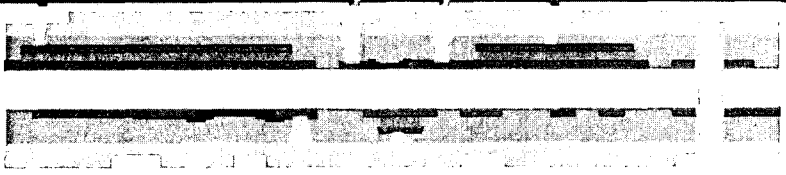
EP Manufacturing Process Flow



EP PWB complete

Process Steps

1. Start with Cu-clad inner-layer
2. Roller coat CFP
3. Laminate Cu foil
4. P & E top Mez. plate
5. Photo-define CFP
6. Print and etch inner-layer; black oxide
7. Apply stability promoter
8. Screen print PTF resistors
9. Laminate RCC
10. Drill MVH and PTH
11. Electroplate outer-layer
12. Circuitize OL & apply SM

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Commercial_ Dupont (I)

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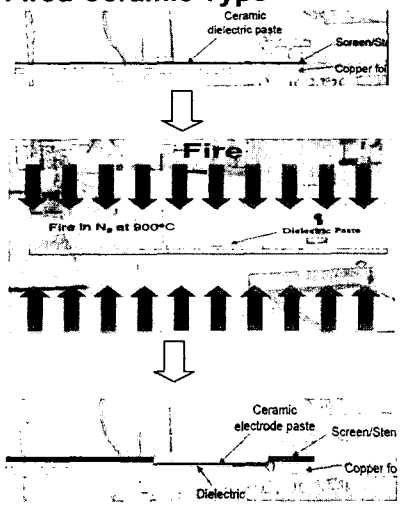
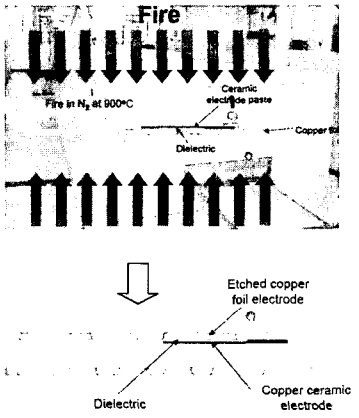
- Fired Ceramic Type





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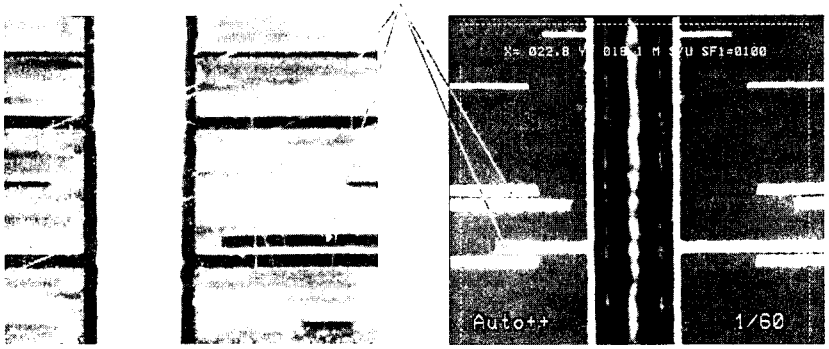
Commercial_ Dupont (II)

37

- **Polymer Type**

DuPont Interra™ HK11

14 micron filled polyimide-based laminate



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Commercial_ Sanmina

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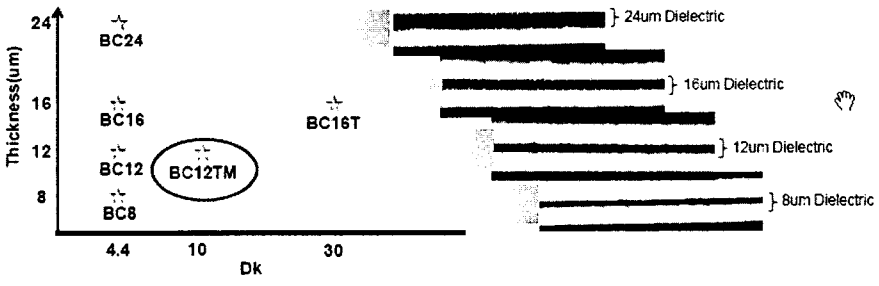
FARADFLEX® BCXX series Material Characteristic data

Properties	Method IPC or others	*FARADFLEX*™ BC24	BC16	BC12	BC8	BC12TM	BC16T
Dielectric Thickness, mm	Nominal	24	16	12	8	12	16
Cp@ 1MHz, nF/in²(pF/cm²)	IPC TM-650 2.5.5.3	1.0 (155)	1.6 (250)	1.9 (300)	3.1 (480)	4.5 (700)	11 (1700)
Dk @1MHz	IPC TM-650 2.5.5.3	4.4	4.4	4.4	4.4	10	30
Loss Tangent @ 1 MHz	IPC TM-650 2.5.5.3	0.015	0.015	0.015	0.015	0.019	0.019
Peel Strength, kN/m	IPC TM-650 2.4.9	>1.0	>1.0	>1.0	>1.0	>0.7	>0.7



KE-TI

Commercial_ Sanmina

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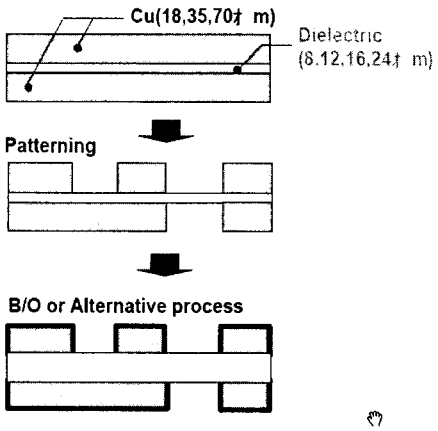
Processing guideline

1. **Pre-clean**
   - Standard process
2. **Expose Image**
   - Standard process
3. **Dry Film lamination**
   - Standard process
4. **Pattern etching**
   - Thin core compatible line recommended
     Ex) Thin core Schmid etching line
   - Use leader board if not confident
   - Careful Handling required
5. **Black oxidizing or alternative oxides**
   - Thin core compatible line recommended
   - Use leader board if not confident
   - Horizontal line preferred
   - Careful Handling required

Important



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Under Development_KAIST

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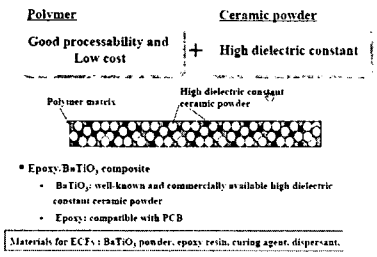

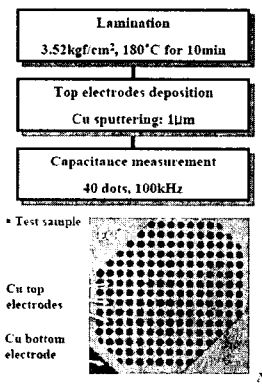

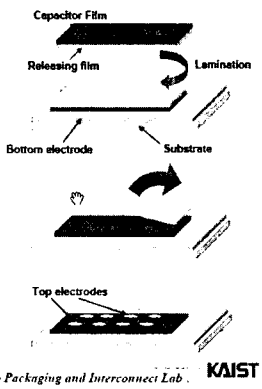

Nano Packaging and Interconnect Lab. KAIST

KE-TI

Under Development_ GIT

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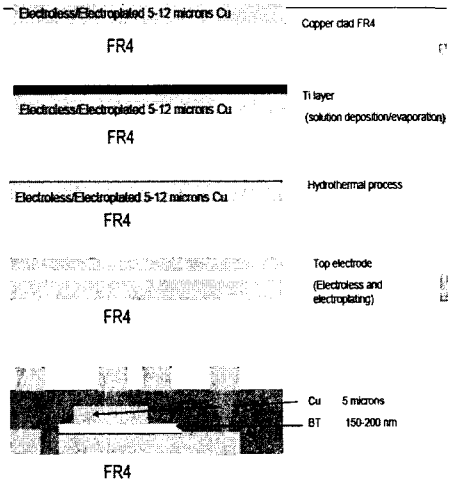
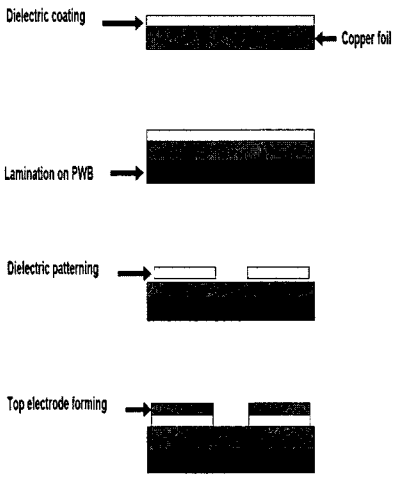
Hydrothermal Process



Sol-gel Process



KE TI

Application -ITRI

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"Embedded Passives on Multilayer Printed Wiring Board for 5 GHz Front-End Module"

<u>Industrial Technology Research Institute, Taiwan</u>

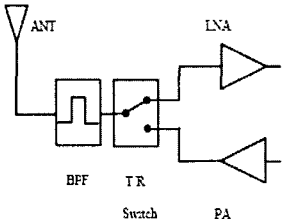


Fig. 1 Block diagram of the RF front-end module

Fig. 3 Coating process for RCC type substrate material

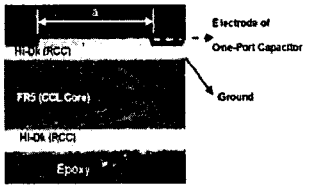


Fig. 6 Cross Section of 1-port Embedded Capacitor

Fig. 19 Photograph of the SPDT switch

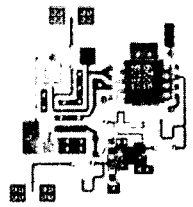


Fig. 15 Photograph of the WLAN PA module

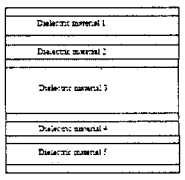


Fig. 2 PCB Substrate structure

Layer	Material	Thickness
Metal 1~6	Copper foil	0.7~1 mil
Dielectric material 1	DK=3.2, DF=0.03	4 mil
Dielectric material 2	DK=65, DF=0.04	2 mil
Dielectric material 3	FR4, DK=3.2, DF=0.02	20mil
Dielectric material 4	DK=65, DF=0.04	2 mil
Dielectric material 5	DK=3.2, DF=0.03	4 mil

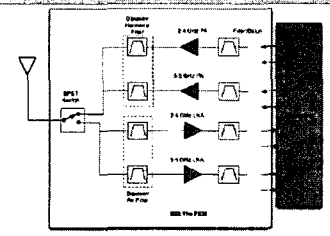
Table 1 Material characters of substrate

ECTC 2006

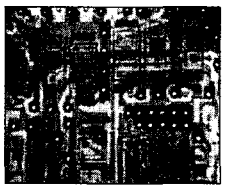
KE TI

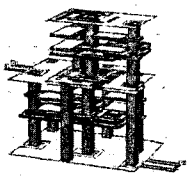
Application -JMD

Design and Implementations of RF Systems and Sub-systems in LCP-type Multilayer Technology"

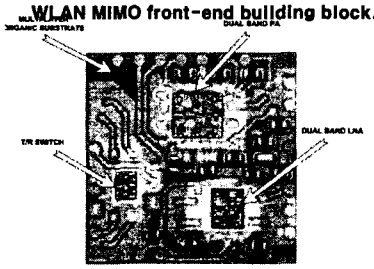


Jacket Micro Devices

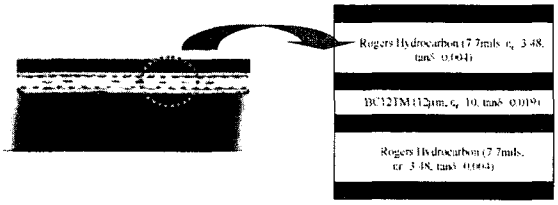




WLAN MIMO front-end building block.



Assembled 1x1 MIMO FEM

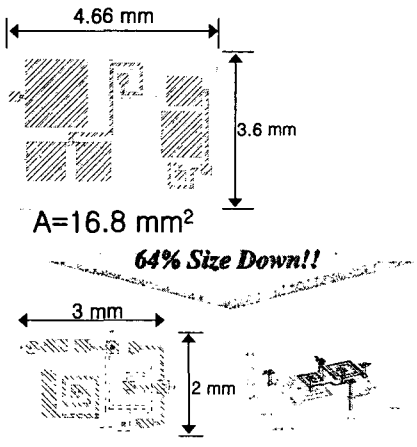


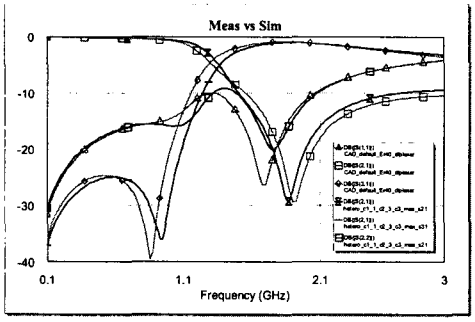
ECTC 2006

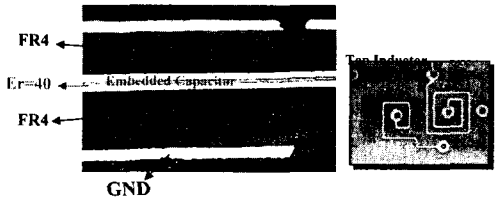
KETI

Application -KETI

- Diplexer:FR4+ Er40 material (Hitachi)







KETI

Future Roadmap in Multilayer

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EPD 소재개발 Roadmap

	2005~2007	2008~2010	2011~2013
재료	EPD for Rigid PCB	EPD for Flex PCB	Ink-jet processing EPD for Flex PCB
	• EC, ER, EL composite • Low loss substrate • Rigid buried passives	• EC, ER, EL composite • Conducting polymer • CP + metal filler • Low loss substrate	• Ink comp. EC/ER/EL • Conductor Ink : CP+ metal filler
공정	Single lamination of Rigid EPD-PCB	Flexible EPD-PCB process	wearable devices
제품	High speed SIP/SOP	Embedded RF module & SOP	Flexible EPD device

*KETI EMPRC

KE-TI

Buried Active by Build-UP

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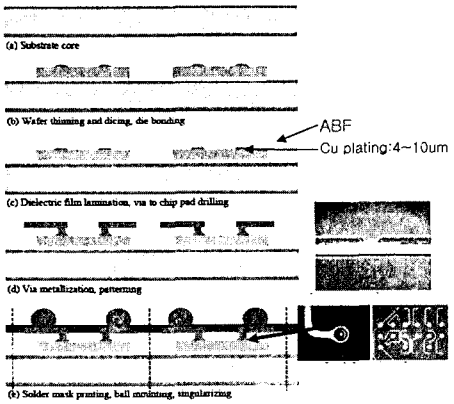
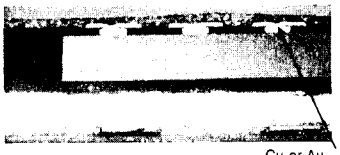
ITRI: CiSP
(chip in substrate Package)



* 2006 ECTC

Wafer grinding(50~60um) 후 Die BondingAl chip Crack발생

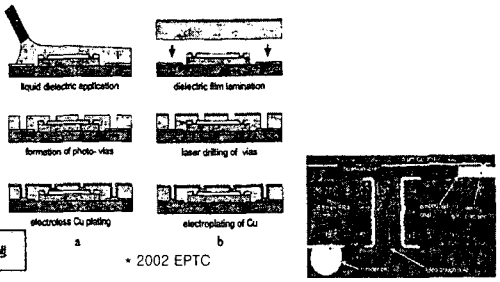
IBM-R



* 2005

Cu or Au
Bump :20~25um

IZM & TUB: CIP
(Chip In Polymer)



* 2002 EPTC

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Buried Active by Build-UP

47

IZM & TUB: CIP
(Chip In Polymer or Hidden Die)

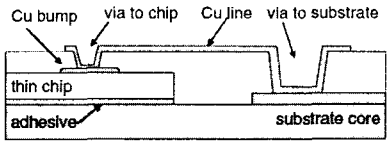
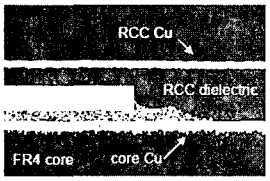


Fig. 1: Interconnect principle of an embedded chip in PCB build-up layer.



2. 5: Embedded chip in a RCC layer.

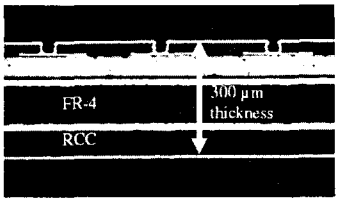


Fig. 3: Chip embedded in a substrate with thin core (via metallisation only by electroless Cu).

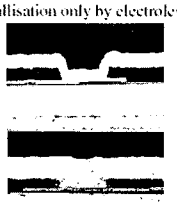


Fig. 6. Microvias to embedded chips metallized with electro less plating and (a) DC electroplating (b) reverse pulse plating

KE TI

Buried Active by Laminate

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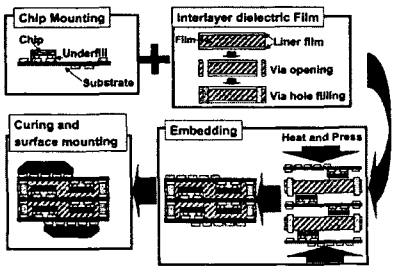
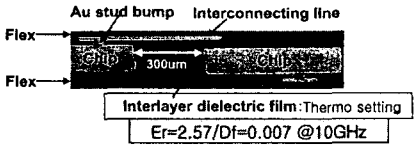
Nitto Denko





* 2004 ECTC

SHIFT (European Union funded prj.)

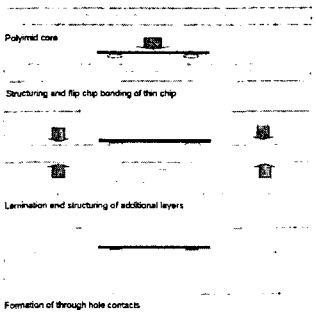
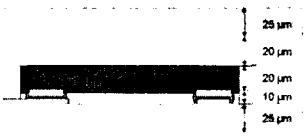


Fig. 9: Schematic process flow of embedding of thin chips into a flexible wiring board.



KE TI