CPFSK communication 사용한 915MHz ISM Band 위한 PLL Frequency Synthesizer 설계

Design of PLL Frequency Synthesizer for a 915MHz ISM Band wireless transponder using CPFSK communication

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Abstract - In this paper, the fast locking PLL Frequency Synthesizer with low phase noise in a 0.18um CMOS process is presented. Its main application is for the 915MHz ISM band wireless transponder upon the CPFSK (Continuous Phase Frequency Shift Keying) modulation scheme. Frequency synthesizer, which in this paper, is designed based on self-biased techniques and is independent with processing technology when damping factor and bandwidth fixed to most important parameters as operating frequency ratio, broad frequency range, and input phase offset cancellation. The proposed frequency synthesizer, which is fully-integrated and is in 320M ~ 960MHz of the frequency range with 10MHz of frequency resolution. And its is implemented based on integer-N architecture. Its power consumption is 50mW at 1.8V of supply voltage and core area is 540㎛ x 450㎛. The measured phase noises are -117.92dBc/Hz at 10MHz offset, with low settling time less than 3.3μs.

Key Words : Frequency Synthesizer, ISM band, CPFSK communication, Integer-N, phase noise

1. Introduction

The explosion of the digital communication market which consist of wireless local-area networks, cordless telephony, cellular, and PCS applications has driven the demand for potable communication systems. These have the common requirement of a low-cost, low-power, small form-factor transponder. This requirement has gradually become widely accepted constraint to design wireless communication system. The cost of CMOS wafer is cheaper than another. And also RF/analog and digital integration is only available in CMOS process.

This paper is focused to the 915M ISM band wireless transponder using CPFSK communication scheme in CMOS process integration.

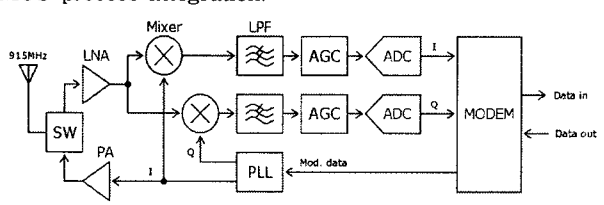

Fig.1 Block diagram of 915MHz CPFSK

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The detailed application block diagram is shown in Fig.1.

2. Frequency Synthesizer Architecture

The frequency of oscillators in RF transceivers must be defined with very high accuracy. The frequency must be varied in small, precise steps. Thus, the error in the output frequency must remain below a few hundred hertz. The architecture that uses an Integer-N divider can be simply shown by using a block diagram like Fig.2.

In the integer-N architecture, the loop bandwidth is limited because the input reference frequency must be equal to the channel spacing.

This, in turn, results from the property that the output frequency are changed by only integer times of F_{REF}. Its block diagram is shown as Fig.2. [1]

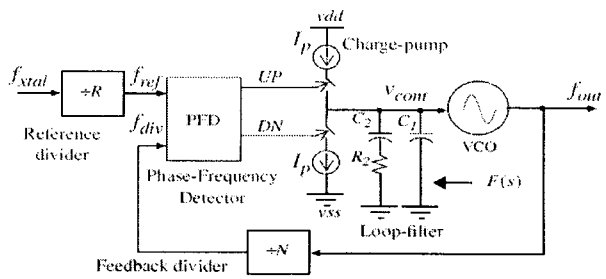


Fig.2 Integer-N Frequency synthesizer

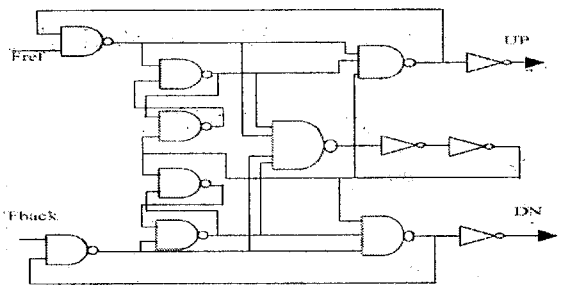


Fig.3. Circuit schematic of the CML_PFD

3. Circuit Design

3.1 CML Phase Frequency Detector

A common architecture for clock generation uses a phase frequency detector (PFD) to simultaneously obtain the phase and frequency. A PFD can monitor the difference between the reference frequency (F_{ref}) and the voltage-controlled oscillator output (F_{back}), and generates either the "up" signal (UP) when F_{ref} leads F_{back}, and the "down" signal (Down) when F_{ref} lags F_{back}. The most desirable feature of a PFD is to have zero dead-zone, which responsible for increasing phase noise and spurious tones. Dead-zone is happened either when the PFD detects zero phase error, or when phase error is present. Zero dead-zone implies that the PFD can detect any amount of phase error. A CML(current mode logic) structure is used to reduce the switching noise and power supply noise. The CMOS logic has the advantage of low power consumption at low frequency operation. The CML requires two lines for each signal.(Fig.3) [2]

3.2 Zero - Offset Charge Pump and Loop filter

A simplified schematic for the zero-offset charge pump is shown in Fig.6. The charge pump is composed of two NMOS source coupled pairs each with a separate current source and connected by a current mirror made from symmetric load elements. Charge will be transferred from or to the loop filter connected to the output when the UP input UP input or DN inputs, respectively, is switched high. With both the UP and DN inputs asserted, the left

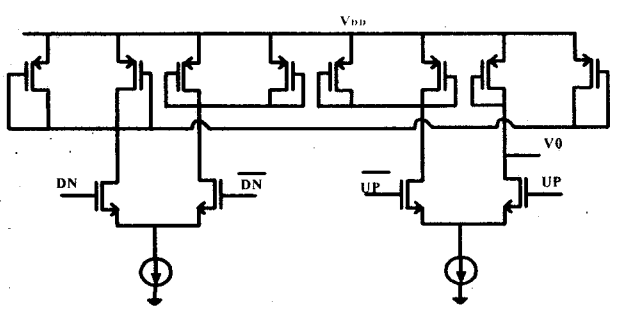


Fig.4. Offset-cancelled Charge Pump with complete schematic

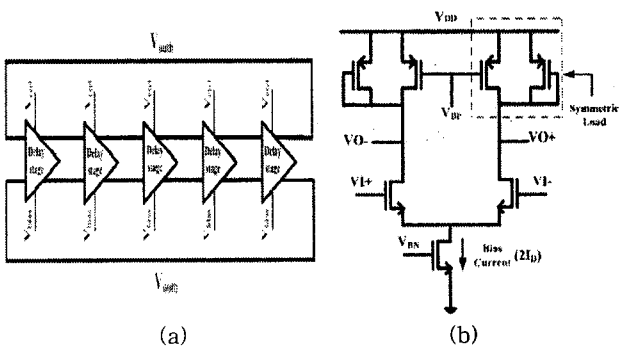
source-coupled pair will behave like the half-buffer replica in the bias circuit and produce V_{CTRL} at the current mirror node. The PMOS device in the right source coupled pair will have V_{CTRL} at its gate and drain which is connected to the loop filter.[3]

3.3 Multiple-pass ring VCO and Programmable Divider

The voltage controlled oscillator (VCO) is perhaps the most crucial element of the frequency synthesizer because it directly provides the output signal of the frequency synthesizer. (Fig.5(a)) The buffer stage, shown Fig.5(b), contains a source coupled pair with resistive load elements called symmetric loads. Symmetric loads consist of a diode-connected PMOS device. The PMOS bias voltage V_{BP} is nominally equal to V_{CTRL}, the control input to the bias generator.[4]

Spectre simulations of the oscillator predicted an operation range of 915MHz for control voltages of 0.75~1.12 V. The measured output was from 320MHz up to 961MHz with tuning gain of 1.72GHz/V.

The design of the dual-modulus pre-scaler itself has been extensively treated in the literature. Here, a program counter acts as coarse tuner and a Programmable counter 'A' as fine tuner. The counter/divider M is given as: M = (N+1) A + N (P - A) = NP + A.



(a) (b)

Fig.5 Multiple-pass ring VCO and delay stage with symmetric loads

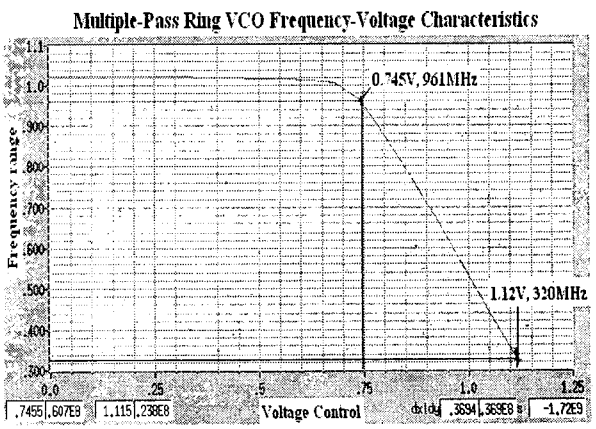


Fig.6. Frequency voltage characteristics of ring VCO

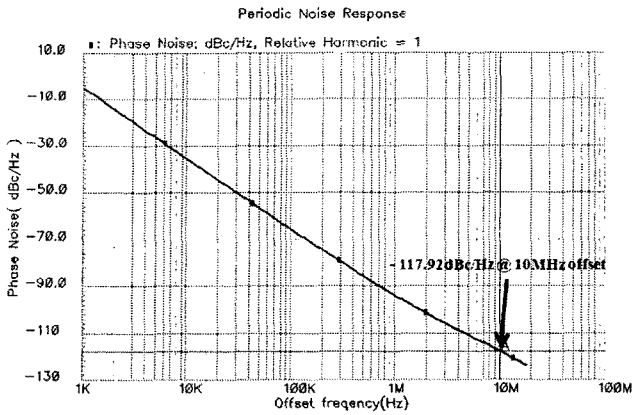


Fig.7. Phase noise characteristics of ring VCO

4. Simulation Result

The simulation result of controlling voltage of VCO, which the locked frequency jumps from 915MHz with the reference frequency at 25MHz, is shown in Fig.8. The flat curve region near 3.3us denotes the locked frequency point, 915MHz, respectively. Fig.9 shows the layout of the fully integrated frequency synthesizer with a chip area of 540μm x 450μm. The power supply is 1.8V. Table I summarizes the performance of the proposed frequency synthesizer.

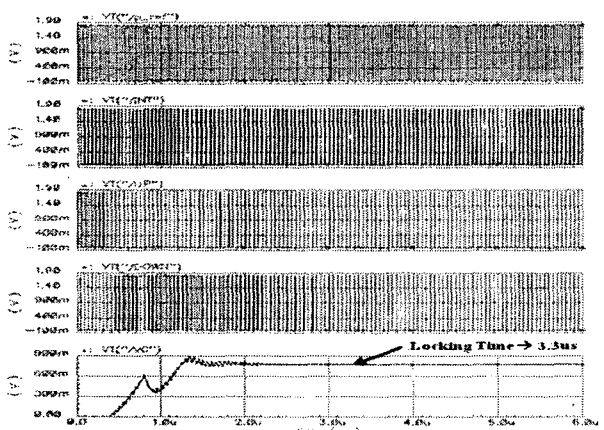


Fig.8. Simulated waveforms of proposed frequency synthesizer

Table I . Performance Summary

Technology	**0.18μm CMOS**
Supply Voltage	**1.8 V**
Frequency Range	**320MHz ~ 960MHz (Kvco = 1.72GHz/V)**
Division ratio	**40 ~ 50**
Core size	**540μm x 450μm**
Phase Noise	**- 117.92dBc/Hz @ 10M offset**
Power Consumption	**50 mW**
Lock Time	**3.3 μs**

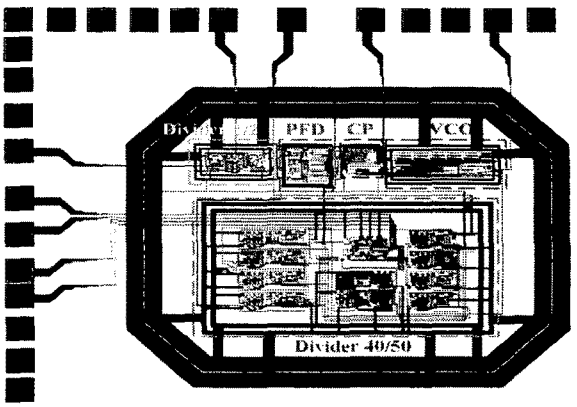


Fig.9. Layout of the frequency synthesizer for a 915MHz ISM

5. Conclusion

In this paper, we proposed the fast locking PLL frequency synthesizer with the low phase noise for a 915MHz ISM Band and realized in a standard 0.18μm CMOS technology.

Its application is focused on the 915M ISM band wireless transponder using CPFSK communication scheme in CMOS process integration. Designed frequency synthesizer was simulated on the basis of 0.18 μm CMOS process using the Spectre-RF software tools. It consumes 50mW of power at 1.8V. Measured phase-noises are -117.92 dBc/Hz at 10MHz offset. Settling time is significantly low being less than 3.3μs. A core size is 540μm x 450μm.

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References

[1] B.Razavi, "Design of analog CMOS integrated circuits", McGraw-Hill,2001..

[2] Chih-Ming Hung, " A Fully Integrated 1.5-V 5.5-GHz CMOS Phase-Locked Loop" IEEE Journal of solid-state circuit, Vol. 37, NO 4, 2002..

[3] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1723--1732, Nov. 1996.

[4] Liang Dai and Ramesh Harjani, "Analysis and Design of Low-Phase-Noise Ring Oscillators", in ftuc. ACMIIEEE ISLPED, pp.289-294, July 2000.