Software GNSS Receiver for Signal Experiments

*Pavel Kovář[1], Libor Seidl[1], Josef Špaček[1], František Vejražka[1]

[1]Czech Technical University in Prague, Faculty of Electrical Engineering (E-mail: kovar@fel.cvut.cz)

Abstract

The paper deals with the experimental GNSS receiver built at the Czech Technical University for experiments with the real GNSS signal. The receiver is based on software defined radio architecture. Receiver consists of the RF front end and a digital processor based on programmable logic. Receiver RF front end supports GPS L1, L2, L5, WAAS/EGNOS, GALILEO L1, E5A, E5B signals as well as GLONASS L1 and L2 signals. The digital processor is based on Field Programmable Gate Array (FPGA) which supports embedded processor. The receiver is used for various experiments with the GNSS signals like GPS L1/EGNOS receiver, GLONASS receiver and investigation of the EGNOS signal availability for a land mobile user. On the base of experimental GNSS receiver the GPS L1, L2, EGNOS receiver for railway application was designed. The experimental receiver is also used in GNSS monitoring station, which is independent monitoring facility providing also raw monitoring data of the GPS, EGNOS and Galileo systems via internet.

Keywords: GNSS receiver, software receiver, SDR, Galileo receiver.

1. Introduction

The research interests of our team are signal processing and GNSS systems. We have looked for an equipment for reception of the GNSS signal which would enable us to reprogram signal processing. Such kind of equipment was not at the market at that time. After the deep analyses we have decided to build our own GNSS receiver. The project started in 2000 by its definition phase. The requirements on our receiver are as follows:

1. The processing of all GPS, GLONASS, SBAS and Galileo signals
2. High flexibility and rapid implementation of the new signal processing
3. Enough performance for the very complex signal processing

Those requirements can be satisfied by the software defined radio (SDR) architecture. The principal schemas of two possible arrangements of the software defined radio are shown on Figure. 1.

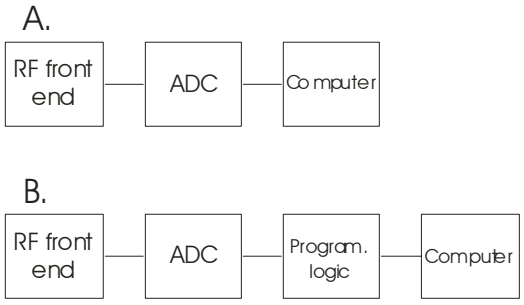

Figure 1. Block diagram of the SDR receiver solutions

The received signal samples in receiver architecture A are directly processed in computer. This laid out high demands on the computer load. This architecture is therefore suitable for processing of signals with the narrower band like GPS L1 signals, in high performance computer like PC workstation, mobile phone or similar devices. The performance of the computer is not mostly sufficient for processing of the wider band signals and therefore the variant B was implemented. The signal samples are firstly processed in the programmable logic device, where the bandwidth of the signal is reduced and then the signal is processed in computer.

In the following paragraph the receiver hardware and software architecture as well as application will be discussed.

2. Experimental GNSS receiver hardware

The hardware of our experimental receiver passes extensive development during this project. Development was caused by the growth of our experiences and fast progress in programmable logic technology and development software.

2.1 First version

The block diagram of the first version of the experimental GNSS receiver is in Figure 2. This receiver consists of three parts: radiofrequency unit, DSP unit and PC workstation.

Radio frequency unit (Fig. 2) consists of two independent radio channels; both channels can operate at any frequency in range 1 – 2 GHz. The bandwidth of each channel is adjustable. Our RF unit supports active and passive GNSS antennas. The gain of the receiver can be controlled either by AGC (Automatic Gain Control) loop, either via external input signal by DSP.

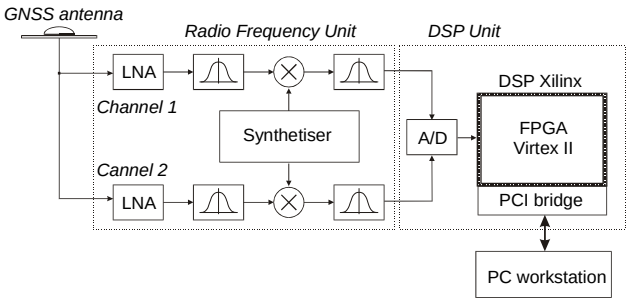

Figure 2. Block diagram of the experimental GNSS receiver

The output signal of radio front end is digitalized and the remaining signal processing is performed in programmable

digital hardware. Digital signal processing is split between FPGA Virtex II by Xilinx and a PC workstation.

The signal processing programmed into the FPGA ensures transformation of the intermediated signal to the base band and correlation reception algorithms. These algorithms have low complexity, but they require high numerical power. The remaining high complexity but less numerical demanding algorithms are executed in PC.

2.2 Second version

The architecture of the second version of the experimental GNSS receiver is very similar to the first version, see Fig. 3. The number of the RF channels has been increased to 4. The frequency plan is slightly changed. The intermediated frequency is increased from 80 MHz to 140 MHz. The main improvement is in the digital part. The advanced FPGA Virtex II Pro by Xilinx with integrated PowerPC processors is applied. This new generation of programmable chip enables to integrate whole high performance embedded computer and signal processing to the single chip. The problem with operation system in the first version of the receiver has been solved by utilization of the real time kernel Micro-C.

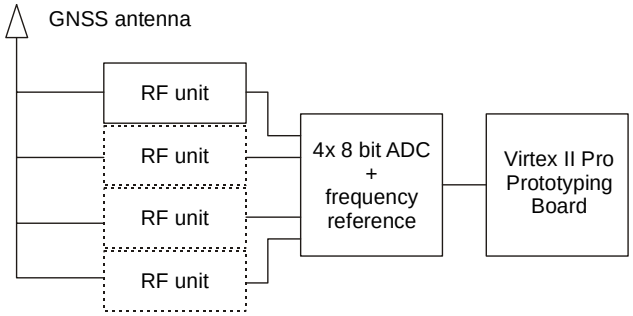

Figure 3. Block diagram of the advanced version of the experimental GNSS receiver

The prototype of the RF unit of the advanced GNSS receiver is in Fig. 4. The main features of this unit are:

Operating frequency	1 – 2 GHz
Intermediated frequency	140 MHz
Unified bandwidth	24 MHz
Automatic gain control (AGC)	>40 dB
External frequency reference	10 MHz

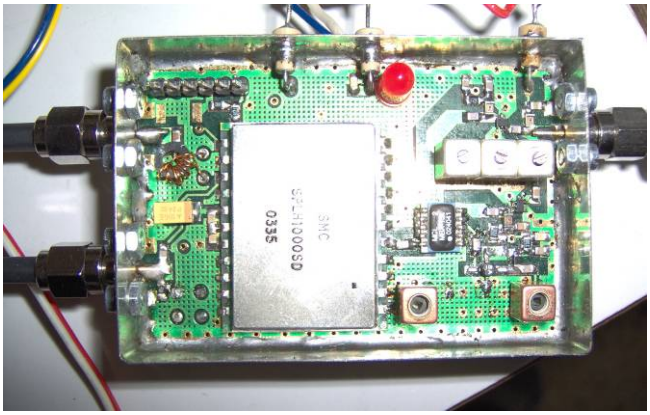

Figure 4. RF unit

The analog to digital converters (ADC) and frequency reference unit is shown in Fig. 5. The main features of this unit are:

8 bit ADC converters	4x
Sampling frequency	80 MHz
Reference frequency	10 MHz
Stability	0.3 ppm
External reference input	
Reference outputs	4 x

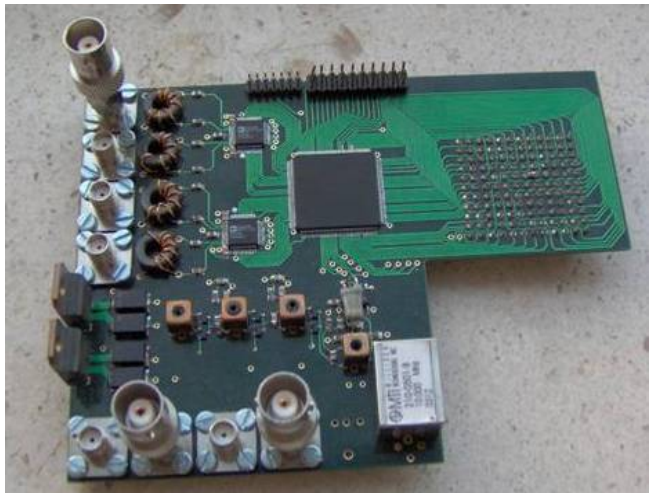

Figure 5. ADC and frequency reference unit

The complete receiver mounted into the 19-inch rack is in the Fig. 6. The Virtex II Pro prototyping board has been used to reduce technological demands for FPGA board development and construction. The receiver is equipped with switched power supplies and high precision frequency reference with stability 0.03 ppm.

Figure 6. Second version of the experimental GNSS receiver in 19-inch rack

2.3. GNSS receiver for railway application

The background and experience obtained during the construction of two versions of the experimental GNSS receiver provided good knowledgebase for construction of a professional GNSS GPS L1/L2 EGNOS GALILEO receiver for railway application based on the second version of experimental receiver. The block diagram of this receiver is shown on Figure 7. Receiver is built on eurocard size (160×100 mm) PCB (Figure 8). The software for this receiver is under development.

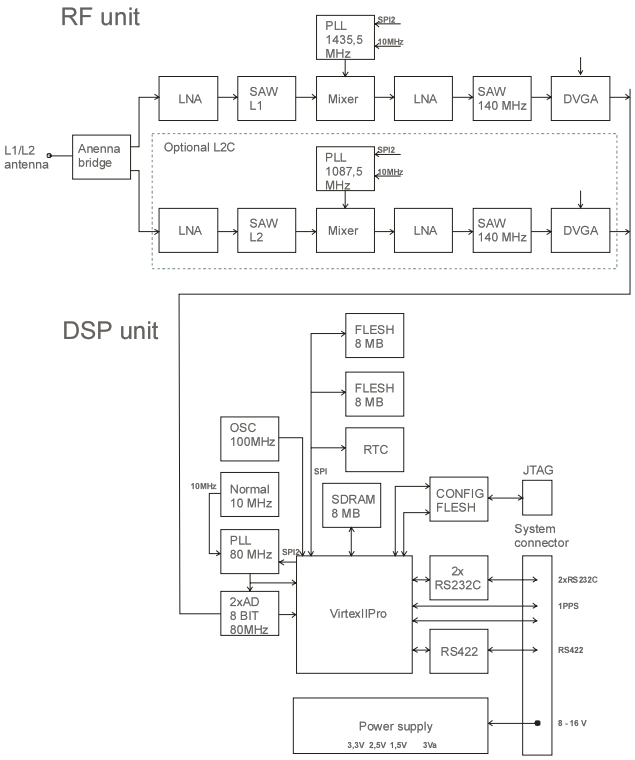

Figure 7. GNSS receiver for railway application - block diagram

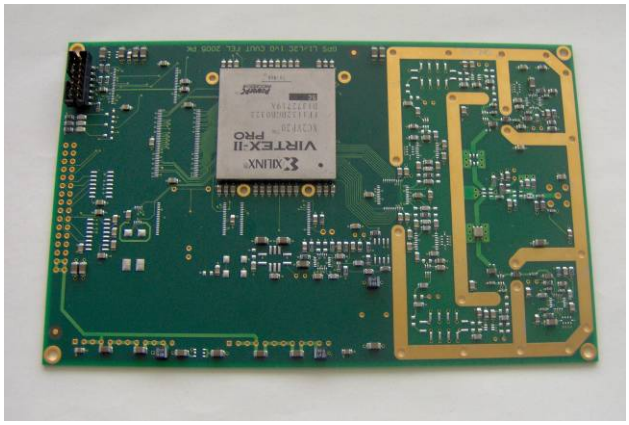

Figure 8. PCB of the GNSS receiver for railway application

3. Applications

Both versions of the experimental GNSS receiver were used for various signal processing experiments. In the beginning phase of this project the correctness of the receiver concept was tested on the GPS L1 CA signal. The receiver was also used for the reception of the Russian GLONASS navigation system.

The experimental receiver was also used for an investigation of the EGNOS signal availability for a land mobile user. The special fast acquisition unit which enables fast response of the receiver on EGNOS signal presence was developed for this project.

The last application of the experimental GNSS receiver is GNSS monitoring station, which is discussed in more details in the next paragraph.

4. GNSS monitoring station

The GPS and GLONASS systems monitoring has long tradition at our department. We continuously monitor those systems and share data via internet since 1996. The development of the GNSS systems and introduction of the new guaranteed services performance requires the development of the GNSS monitoring system. The basic requirements on the provider-independent monitoring system are:

1. Measurement and storage of signal or data on very low level, to be able to reconstruct the anomalous behavior of the navigation system and simultaneously eliminate mistakes in the monitoring system
2. Support the investigation of the anomalous status of the navigation system and secure data for reconstruction of the anomalous behavior of the navigation receiver
3. Support transformation of the low level data and signal to the widely used format for other analyses
4. Share monitoring data via internet.

4.1. GNSS monitoring station architecture

The construction of the GNSS monitoring station is planned in several phases. In the first phase the monitoring station will monitor all in view GPS, EGNOS, and GALILEO satellites on L1 frequency. In the next phase the capability of monitoring of the GALILEO E5, GPS L2 CA, and GPS L5 signals will be progressively implemented.

The basic block diagram of GNSS monitoring station is in Figure 9. Monitoring station consists of the second generation GNSS receiver equipped with the L1 front end. For this purpose the 16 identical GPS/EGNOS/GALILEO correlators capable to process BPSK and BOC(1,1) modulation were programmed to the receiver FPGA. The PRN code is stored in the correlator 16 Kbits RAM memory and can be downloaded from the receiver computer.

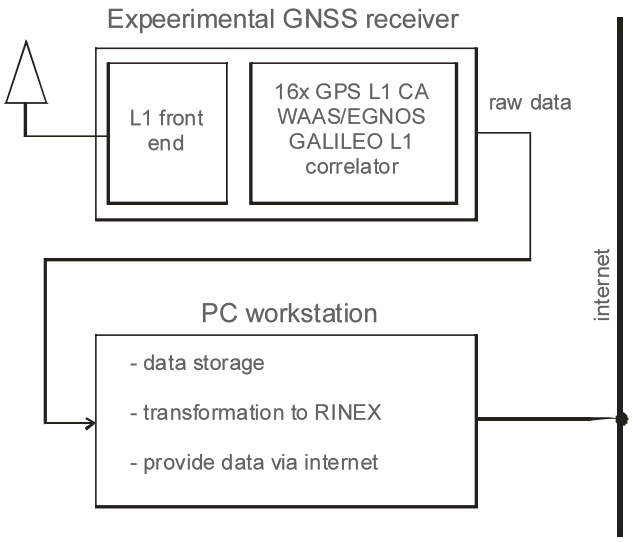

Figure 9. GPS, EGNOS, and GALILEO monitoring station

4.2. GNSS monitoring station data format

The requirements on transparency and capability of the post processing investigation of the non standard system and receiver states were taken in account in development of the data format and communication protocol for GNSS monitoring station. From this reason the monitored data are stored in PC workstation in

raw form to keep available all information for measurement analyses and elimination of the errors in the monitoring station (Table 1.).

Table 1. Monitoring station raw data content

1. Raw carrier phase measurement
2. Extended PLL status - actual tracking error - detailed PLL status indicators
3. Raw code measurement
4. Extended DLL status - actual tracking error - signal to noise ratio - detailed DLL status indicators
5. IQ signal samples wide one bit - 20 ms for GPS - 2 ms for EGNOS - 1 ms for GALILEO

The software for analyses of the measured data and signals and for transformation of this raw data to the RINEX format runs on PC workstation. The PC Workstation also provides this data via internet.

For analyses of the RINEX data can be used some navigation or surveillance software packages like Pegasus software by Eurocontrol for EGNOS.

The other possible way how to analyze the monitored data is to develop special software. This software targeted for Matlab environment is under development. The software will directly process raw data measurement, because RINEX format supports only subset of the raw measurement information.

5. Future plans

In the frame of this project we plan to upgrade GNSS monitoring station to all GALILEO frequencies. The second version of the experimental GNSS receiver has not sufficient performance of the FPGA for implementation of the approximately 100 correlators including GALILEO E5 correlators, which should process extra wideband signals. Our plan therefore supposes the design of the third version of the experimental GNSS receiver based on latest Virtex 4 FPGA by Xilinx with higher performance.

The goal of this receiver is power sufficient for processing of all GALILEO signals in space.

6. Conclusion

The experimental GNSS receiver enables us to realize series of experiments with real GNSS signals which cannot be carried out with the commercial receivers. The architecture of the receiver was approved by many experiments. Main advantage of the receiver is its versatility. The utilization of the modern development tools for FPGA, signal processing, and embedded computers supports rapid implementation of the investigated algorithms to the receiver.

Acknowledgement

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