A Self-Biased Current Reference in 0.25μm CMOS Technology

Jaewoo Park*, Changsik Yoo**
Department of Electronics and Computer Engineering, Hanyang University
E-mail : *wooya00@ihanyang.ac.kr, **csyoo@hanyang.ac.kr

Abstract

A self-biased CMOS current reference is described which provides supply and temperature independent bias current. The supply independency is obtained by subtracting two bias currents which have the same supply dependency. Unlike the conventional self-bias CMOS current reference, excellent supply independency can be obtained even with the minimum channel length devices and thus smaller area implementation becomes possible. The supply independent bias current is then applied to a temperature compensating circuit and as a result supply and temperature independent bias current is obtained. The current reference has been implemented in a 0.25μm standard CMOS technology. The active silicon area is only 45μm×45μm. The simulated temperature coefficient is 64ppm/°C in temperature range between 0°C and 120°C. Supply voltage can be as low as 1.3V and the supply dependency of the current reference is measured to be smaller than 4500ppm/V. While providing 10.25μA output current, the current reference consumes 160μW.

I. Introduction

Current reference is an essential block in analog circuits for biasing purposes. Any variation in the reference current affects the biasing point of other blocks and decreases the accuracy of overall system. Therefore many analog circuits require very stable current source. For this reason, many high precision, PVT (process, voltage and temperature) variation compensated reference circuit has been proposed. However, the circuits that show high performance tend to increase complexity and cost for circuit design.

The purpose of this work is to develop a low cost CMOS current reference circuit that generates the comparable precision reference current with variations of supply voltage and temperature in a simple way. The proposed circuit consists of two parts which compensate both the variation of supply voltage and temperature. Since this current reference circuit is fully compatible with standard CMOS technology and occupies very small area, it can be easily integrated with other CMOS analog or mixed mode system.

II. Circuit design

For supply and temperature independent biasing, usually bandgap reference is employed which requires bipolar transistors. In a standard CMOS process, lateral pnp bipolar transistor can be easily realized but its performance is very poor and more critical concern is the necessity of the accurate modeling of the lateral pnp transistors. Therefore, we have adopted the MOS-only self-biased reference.

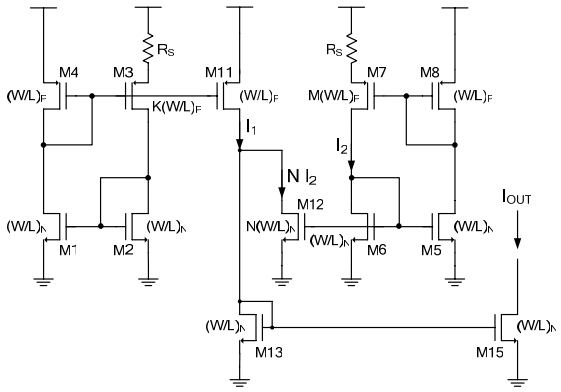

Fig. 1. Supply independent current generation

In order to have sufficient supply independency, two self-biased CMOS current references are built which have the same supply dependency. The difference of the two current outputs I_1 and N I_2 is taken as the output as shown in Fig. 1, canceling the supply dependency of I_1 and N I_2. Since the supply independency can be achieved with minimum channel length

This work was supported in part by the HY-SDR research center under the ITRC program of MIC, Korea. The CAD tools were supported by IDEC.

The authors are with the Department of Electronics and Computer Engineering, Hanyang University, Haeng-Dang-Dong 17, Seong-Dong-Ku, Seoul 133-791, Korea (E-mail : csyoo@hanyang.ac.kr)

devices the required silicon area is much smaller than the conventional CMOS current reference which requires long channel devices.

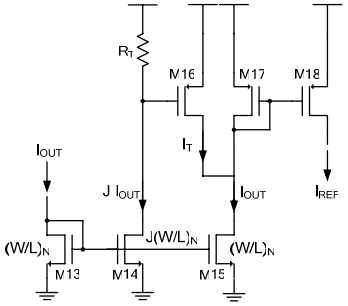

Fig. 2. Temperature compensation circuit.

The temperature coefficient of the supply independent current source in Fig. 1 is positive. In order to get temperature independent output current, the circuit shown in Fig. 2 is proposed. The current I_{OUT} from the supply independent current source is multiplied and converted to voltage by the resistor R_T. For higher temperature, I_{OUT} increases and thus the gate voltage of M16 decreases which results in higher value of I_T. By subtracting the current I_T is subtracted from the supply independent current I_{OUT}, the final output current I_{REF} can have low temperature dependency.

Ⅲ. Experimental results

The proposed CMOS current reference in Fig. 1 is simulated to see the supply dependency whose result is shown in Fig. 3. The minimum operable supply voltage is about 1.0V and the supply rejection is 0.5%/V. The output current can be easily scaled by the area ratios K, M, and N.

The temperature dependency of the current reference is simulated to be 64ppm/^{o}C as shown in Fig. 4.

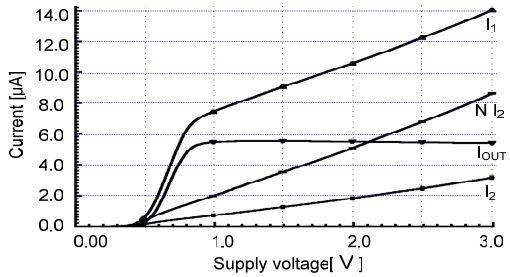

Fig. 3. Simulation results of the supply independent current source in Fig. 2.

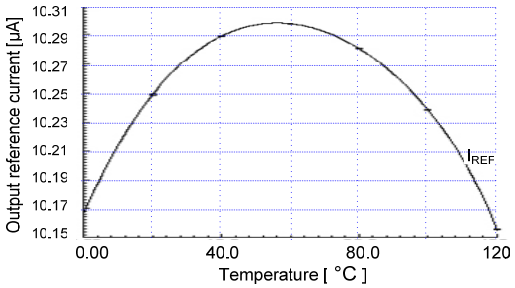

Fig. 4. Simulated temperature dependency

The proposed supply and temperature independent current source has been implemented in a 0.25μm standard digital CMOS process. The current reference occupies very small area of 45μm×45μm. The current reference provides constant output current for the supply voltage higher than 1.3V and its supply dependency is 3000ppm/V for the supply voltage ranging from 1.3V to 2.5V. The current reference consumes 160μW when providing 10.25μA output current.

Ⅳ . Conclusion

A self-biased CMOS current reference is described which provides supply and temperature independent bias current. The supply independency is obtained by subtracting two bias currents which have the same supply dependency. Unlike the conventional self-bias CMOS current reference, excellent supply independency can be obtained even with the minimum channel length devices and thus smaller area implementation becomes possible. The supply independent bias current is then applied to a temperature compensating circuit and as a result supply and temperature independent bias current is obtained. Since this current reference circuit is fully compatible with standard CMOS technology, it can be easily integrated in a CMOS analog or mixed mode system.

Reference

[1] R. J. Baker, CMOS circuit design, layout, and simulation, IEEE press, 2005.

[2] F. Fiori and P. S. Crovetti, “A new compact temperature-compensated CMOS current reference.” *IEEE Trans. Circuits Syst. II*, pp. 724 - 728, Nov. 2005