Reduction of Breakdown Voltage in I-MOS Devices

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1. Introduction

Aggressive scaling-down of MOSFETs has aggravated some important problems [1], [2]. One of them is the reduction of subthreshold swing. Recently, in order to achieve sub-60-mV/dec subthrehold swing at room temperature, some novel devices have been proposed [3]-[5]. Among them, we have focused on the I-MOS (impact-ionization metal-oxide-semiconductor) device [6]-[10]. Its basic structure is illustrated in Fig. 1, which is basically a gated p-i-n diode structure. Since the p-n junction barrier lowering is not the mechanism of current flow control in the I-MOS device, it is possible to reduce the subthreshold swing below 60 mV/dec at room temperature.

In our previous work, we proposed a novel biasing scheme based on device physics to make the I-MOS device more feasible, which leads to negative source voltage [6]. The absolute value of the source voltage is necessary to reduce for the following reasons. Firstly, it helps device reliability. Since the I-MOS device uses an avalanche breakdown as a carrier injection mechanism, generated hot carriers can damage semiconductor-insulator interfacial layer. As the source voltage becomes lower, the energy of hot carriers will also be reduced. Secondly, it contributes to low-power consumption in that static power (P_{stat}) and short-circuit power consumption (P_{dp}) are closely related to the source voltage (V_S) as below [11]:

$$P_{stat} = I_{leak}(V_{out,\max} + V_S) \quad (1)$$

$$P_{dp} = (V_{DD} + V_S) I_{peak} ((t_r + t_f)/2) f \quad (2)$$

where I_{leak}, $V_{out,max}$, f, I_{peak}, t_r, and t_f represent leakage current, maximum output voltage, operating frequency, maximum crowbar current, rise time, and fall time, respectively.

In this paper, we propose and confirm two approaches to reduce the source voltage: shallow source extension formation and strained SOI (silicon-on-insulator) technology. The former is easy to apply but its effect is limited. On the other hand, the latter is the opposite case. Simulated device structure referred to that in Ref. [9] and Selberherr's model [12] was selected for impact ionization model.

2. Shallow Source Extension Formation

In Ref. [8] and [9], we proposed a novel I-MOS device structure which features the source extension region. It consists of plane and cylindrical region as depicted in Fig. 2. When a p-n junction is formed by implantation or diffusion through a window in a mask layer, the dopants will diffuse downward and also sideways. It has been reported that this cylindrical region has critical effects on junction, especially for the avalanche breakdown process [13]. As the junction depth of the source extension is reduced, the radius of curvature of the cylindrical region decreases and finally the voltage necessary for inducing avalanche breakdown also decreases [14]. This reduction of avalanche breakdown voltage has no apparent theoretical limit [15]. A continuous decrease in the radius of curvature leads to a continuous decrease of the breakdown voltage until other breakdown mechanisms dominate and carrier multiplication is therefore no longer an important factor. We investigated the relationship between the junction depth of the source extension region and the source voltage by device simulation. Fig. 3 shows that the threshold voltage and the source voltage to maintain constant threshold voltage strongly depend on the junction depth of the source extension region. Thus, if state-of-the-art shallow junction technologies are used, the source voltage is expected to be further reduced.

3. Strained SOI Technology

Fundamental solution of the source voltage reduction is to use small-bandgap material because threshold energy (E_i) which is defined as minimum energy required for impact ionization is closely related to the bandgap energy. Since the bandgap energy of silicon is quite large (1.12 eV), germanium whose bandgap energy is 0.66 eV has been thought of as a promising alternative [3]. However, there are still many technological barriers to make germanium process practical [16]. Thus, in this paper, we investigated the feasibility of strained silicon technology to reduce the bandgap. Strained silicon is one of the key technology boosters in modern CMOS technology. Its main advantage is enhanced carrier mobility.

However, in this paper, our interest is confined within the bandgap variation as a function of strain. It has been widely known that lattice strain alters the band structure of a semiconductor by shifting it in energy, distorting it, and removing degeneracy effects [17]. In simulation, we refer to the bandgap of strained silicon or SiGe on a relaxed Ge (100) buffer layer in Ref. [18] and [19]. For simple simulation, we assumed E_i to be proportional to bandgap energy, which is reasonable according to Ref. [20]. Fig. 4 shows that source voltage can be reduced down to -1.28 V in the case of silicon layer grown on a Ge (100) buffer layer, which is much lower than -2.22 V in pure germanium case. In addition, we have already confirmed that an SOI wafer is preferable to a bulk one in terms of leakage current control [9]. Therefore, when using strain engineering, a strained SOI wafer will be appropriate..

4. Conclusions

We have proposed two ways of reducing the breakdown voltage of I-MOS devices and confirmed them by device

simulation. Though both of them were effective, strained SOI technology showed the feasibility of abrupt breakdown voltage reduction in spite of difficulty in fabrication.

Acknowledgements

This work was supported by the BK21 program and by the Nano-Systems Institute (NSI-NCRC) program sponsored by the Korea Science and Engineering Foundation (KOSEF).

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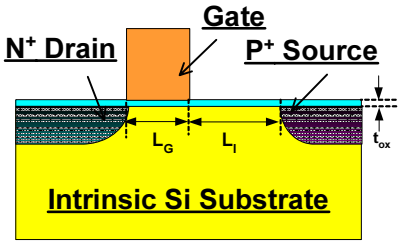

Fig. 1. Basic device schematic of the n-channel I-MOS device.

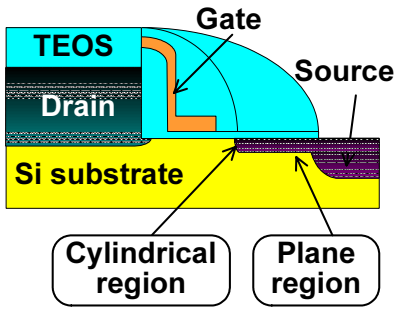

Fig. 2. Plane and cylindrical region of the source extension region.

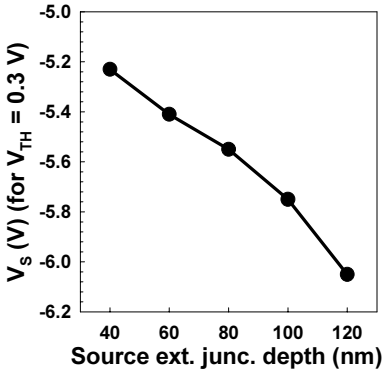

Fig. 3. Dependence of the source voltage on the junction depth of the source extension region.

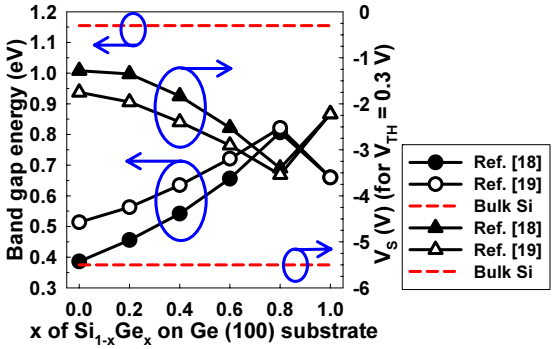

Fig. 4. Source voltage reduction as a function of strain.