Design and Simulation of Asymmetric MOSFETs

Jong Pil Kim, Woo Young Choi, Jae Young Song, Sang Wan Kim, Jong Duk Lee, and Byung-Gook Park
Inter-University Semiconductor Research Center
and School of Electrical Engineering and Computer Science, Seoul National University,
San 56-1, Sillim-dong, Gwanak-gu, Seoul, 151-742, Korea
Tel: +82-2-880-7282, Fax: +82-2-882-4658, e-mail: jpkim78@snu.ac.kr

1. Introduction

MOSFET scaling has been accelerated thanks to its excellent performance and scaling properties. However, as the size of the device is reduced down to deep sub-micron region, it suffers from some critical problems [1],[2]. One of them is breakdown at the edge of drain. Breakdown occurs in a short-channel MOSFET when the drain voltage exceeds a certain value. When the field exceeds mid-10^5 V/cm, impact ionization takes place at the drain, leading to an abrupt increase of drain current. It can be relieved to some extent by using a lightly doped drain (LDD) structure, which reduces the peak field in a MOSFET [3]. However, the drain current is reduced due to the parasitic resistance in the LDD region. Because of the recent industry emphasis on high-speed technology, it is critically important to optimize the LDD design for maximum current-drive capability while maintaining acceptable hot-carrier reliability [4]. One way to optimize LDD design is the use of asymmetric LDD (with no LDD on the source side) structures. Asymmetric LDD devices have been studied in the device level for 0.5 µm technology.[5],[6] As MOS devices are scaled to deep sub-micrometer regime, parasitic resistance in the LDD region may impose a greater detrimental effect to the driving current. We have decided to examine the asymmetric LDD structure of MESA type with 25 nm channel length using sidewall spacer and compare it with conventional LDD device

In this work, we compare device performances between 25-nm asymmetric and symmetric NMOSFET using device simulator (SILVACO).

2. Device Structures

Fig. 1 shows the cross section of 25-nm asymmetric NMOSFET used in device simulation. As mentioned before, in order to increase drain current, we remove LDD region at the source and we introduce a mesa shape to reduce both the drain influence on the source and channel length by using a sidewall spacer.

At first, for the source implantation, we have implanted arsenic into the p-type [100] bulk silicon wafer and then the source region is defined in a mesa shape. But it is not easy to control junction depth. So we have simulated source implantation energies by splitting hem into three types to make the junction depth of the source similar to the height of the source. After channel doping for threshold voltage adjustment, gate oxide (t_{ox}=2 nm) is formed using thermal oxidation and the sidewall spacer gate is formed next to the source. Poly-silicon thickness is very important because it determines the channel length. We have doped the LDD region with low energy and then a TEOS sidewall spacer is formed for high energy drain implantation in order to minimize the drain parasitic resistance. In the final step, annealing process activates impurities with minimized diffusion

Fig.2 shows the device structures of 25-nm asymmetric and symmetric NMOSFETs. Symmetric NMOSFET has the same physical parameters and channel length.

3. Results and Discussions

The I_D-V_G characteristics of symmetric and asymmetric NMOSFETs are shown in Fig. 3. In case of the symmetric NMOSFET, the threshold voltage (V_{TH}) is -0.05 V and the sub-threshold swing (SS) is 176 mV/dec at V_{DS}=0.05 V. For the asymmetric NMOSFET, the threshold voltage and sub-threshold swing are 0.1 V and 100 mV/dec, respectively. Drain-induced barrier lowering (DIBL) is 120 mV/V. I_{ON} and I_{OFF} are obtained at V_G–V_{TH}=0.8 V and V_G–V_{TH}=-0.2 V, respectively. The results of simulation are summarized in Table I. The asymmetric NMOSFET has small SS and DIBL as well as high ON/OFF current ratio in comparison with the symmetric NNOSFET as shown Fig. 3. The device structure which we proposed has immunity against the short channel effects of planar MOSFETs. The driving current of the asymmetric NMOSFET is higher than that of the symmetric NMOSFET because the parasitic resistance of source region is decreased by removing LDD at the source side. In other words, removing LDD from the source side results in much less voltage drop in the source-side LDD region. So, we can expect that the asymmetric MOSFET would be operated at lower V_{DD}. Furthermore, OFF current of the asymmetric NMOSFET is less than that of the symmetric one because the depletion profile of the asymmetric NMOSFET between source to body is different from that of the symmetric one.

The I_D-V_D characteristics of the symmetric and asymmetric NMOSFET are shown in Fig. 4.

Two interesting results are observed in Fig. 4. First, when drain voltage(V_{DS}) was swept from 0 V to 1.2 V at V_G=0 V, the drain current of the symmetric NMOSFET increases very slowly as seen in Fig 4, while that of the asymmetric NMOSFET at the same conditions exhibits constant point(I_D = 0 A). This difference can be explained in the following way. In case of the symmetric NMOSFET, the depletion region at the drain side is increased when the drain voltage is applied from 0 V to 1.2 V, so that punch-through phenomenon takes place. However, the asymmetric NMOSFET which has an elevated source results in much less punch-through phenomenon than the symmetric one because the profile of depletion region is different.

As seen in Fig. 4, the other interesting observation is that the linear region of drain current curve at V_G=1 V does not increase when we compare it with V_G=0.5 V. This results imply that the resistance is very large. But the resistance of the asymmetric NMOSFET as seen in Fig. 4 shows different situation. Finally, by removing LDD region of source side, parasitic resistance decreases, so that drain current increases.

5. Conclusions

We have introduced an asymmetric NMOSFET of MESA structure with no LDD on the source side. This structure has merits in terms of device scaling down and device performance.

First, this structure can control channel length by using sidewall spacer and implement self-alignment. In addition, this structure can increase driving current by removing LDD region in the source side.

The performance of the asymmetric NMOSFET was examined. Compared with symmetric NMOSFET through the device simulations, the asymmetric one exhibits higher I_{ON}. The SCE of the proppsed device is more effectively suppressed than that of the conventional MOSFET.

Acknowledgements

This work was supported by BK21 programs, by the Nano-Systems Institute (NSI-NCRC) program sponsored by the Korea Science and Engineering Foundation (KOSEF).

References

[1] M. Lundstrom, *IEEE Int. Electron Devices Tech. Dig.*, pp. 789-792, 2003.
[2] W. Y. Choi *et al*, *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 210-216, Dec.2003.
[3] Yuan Taur *et al*, Fundamentals of Modern VLSI Devices.
[4] Jone F. Chen *et al* , *IEEE Journal of Solid-State Circuits*, vol. 34, no. 3, pp. 367-371, Mar. 1999.
[5] T. N. Buti *et al*, *IEDM Tech. Dig.*, pp. 617-620, 1989
[6] T. Horiuchi *et al*, *IEEE Trans. Electron Devices*, vol. 41, no. 2, pp. 186-190, 1994.

Table I. Results of device simulations.

	Symmetric NMOSFET	Asymmetric NMOSFET
V_{TH} (V)	-0.05	0.1
I_{ON} (μA/μm)	420	668
I_{OFF} (μA/μm)	4.25	0.475
SS (mV/dec)	176	100
DIBL (mV/V)	180 ~ 200	120

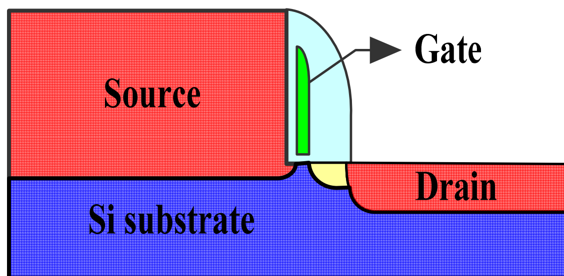

Fig. 1 Cross-section of 25-nm asymmetric NMOSFET used in this simulation work.

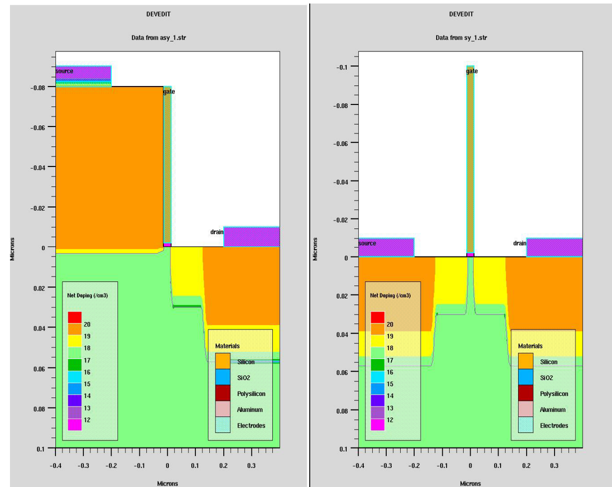

Fig. 2 Device structures of 25-nm asymmetric and symmetric NMOSFET. Basically this structures have the same physical parameters.

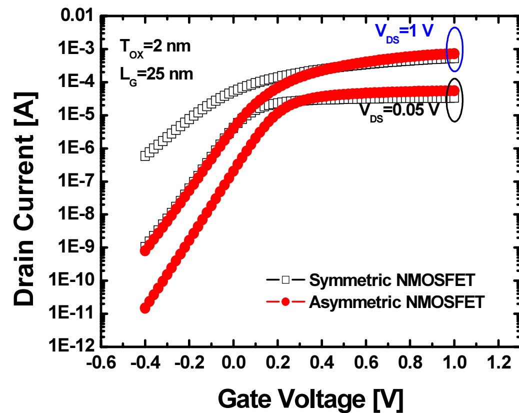

Fig. 3 I_D – V_G characteristics of the symmetric and asymmetric NMOSFET. The asymmetric device has smaller SS and DIBL as well as high ON/OFF current ratio than symmetric device.

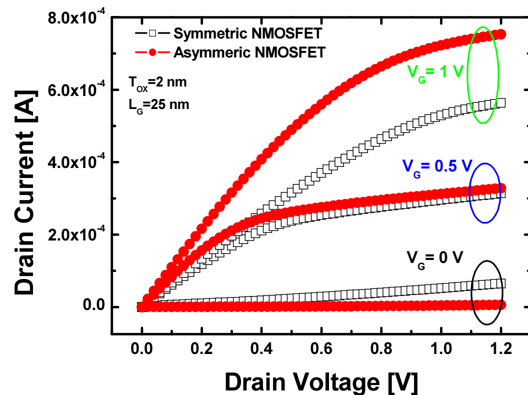

Fig. 4 I_D – V_D characteristics of the symmetric and asymmetric NMOSFET. The latter shows higher conductance value than the former.