Electrical properties of Organic TFT patterned by shadow-mask with all layer

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Abstract

Pentacene thin film transistors fabricated without photolithographic patterning were fabricated on the plastic substrates. Both the organic/inorganic thin films and metallic electrode were patterned by shifting the position of the shadow mask which accompanies the substrate throughout the deposition process. By using an optically transparent zirconium oxide (ZrO_2) as a gate insulator and octadecyltrimethoxysilane (OTMS) as an organic molecule for self-assembled monolayer (SAM) to increase the adhesion between the plastic substrate and gate insulator and the mobility with surface treatment, high-performance transistor with field effect mobility 0.66 cm^2 /V s and I_{on} / I_{off} >10^5 was formed on the plastic substrate. This technique will be applicable to all structure deposited at low temperature and suitable for an easy process for flexible display.

1. Introduction

In this study, we will present a technique for improving performance of an organic thin film transistor (TFT) using the shadow-mask process. We formed the OTMS on a hydrophilic ZrO2 surface so that the long alkyl tails form a tightly packed monolayer while the Si adheres to the surface of ZrO2 through Si–O covalent bonds [1-2].

2. Experimental

Polyethersulfone (PES) films are used as flexible substrates. After curing of PES to eliminate the minute pin-holes for 60 min at 120 C, Au of 80 nm thick as a gate electrode was thermally evaporated by using a shadow-mask under vacuum of less than 2 x10^{-6} Torr. On the patterned gate electrode, a 250-nm-thick ZrO_2 for gate dielectric layer was deposited by the e-beam at relatively low temperature (<120 °C). Following the gate dielectric layer deposition, in order to have a good affinity of organic molecule on the surface of the dielectric layer, we modified the surface of ZrO_2 by using combinational SAMs of alkyl silanes. The SAMs deposition was performed by soaking a solution of OTMS/isopropanol (1:20/v:v) for 2–3 min under nitrogen atmosphere. Source and drain electrodes were aligned by the shadow mask aligner consisting of 100 nm Au and were deposited onto the gate dielectric layer using thermal evaporation. The channel length L is 200 μm and width W is 1000 μm. Pentacene as an active layer was grown by vacuum evaporation at a working pressure of 6x10^{-6} Torr. During the pentacene deposition, the substrate temperature was held at 60 ℃. The thickness of pentacene film was 100 nm with a deposition rate of 1 Å/s. Electrical measurements were performed at room temperature in air by using a parameter analyzer (HP4145, Hewlett-Packard). Capacitance measurements of the ZrO2 were carried out by using a C-V analyzer (Keithly).

3. Results

Figure 1 presents the capacitance-voltage (C-V) characteristics of Metal-Insulator-Si (MIS) structure in order to acquire the dielectric characteristics of ZrO_2. The capacitance was measured as the maximum value of 1 and the minimum value of 0.96 when the applied voltage was increased from -10 V to 10 V. The flat-band voltage of new oxide material was calculated as -0.16 V in the characteristic curve. ZrO_2 is an attractive candidate since it has a high dielectric constant (15-22), a high breakdown field (15-20 MV/cm), a large band gap (5-7 eV) and may be thermodynamically stable on silicon.

The kink phenomena shown in Figure 2 (a) drain current – drain voltage (I_D-V_D) characteristics are attributable to the increased surface potential barrier height between a pentacene organic layer and a gate dielectric layer, resulting in the serious device degradation. Figure 2 (b) drain current – gate voltage (I_D-V_G) curve illustrates the electrical characteristics such as on/off current ratio of 10^4 and the field effect mobility of 0.12㎠/Vs at the drain voltage of –0.1V. However, considering the possible positive effect of the organic molecules modifying the surface of gate

dielectrics, we applied OTMS as the organic molecules on the surface of gate dielectric layer. The OTMS deposited on the ZrO_2 surface was confirmed by Infra-red spectroscopy as shown in Figure3.

Figure 4 (a) I_D-V_D and (b) I_D-V_G show electrical characteristics for the organic pentacene TFTs with a channel width of 1000 ㎛ and a channel length of 200 ㎛ in the presence of the OTMS surface treatment on the gate dielectrics. The mobility increased up to 0.66 ㎠/Vs and the on/off current ratio of 10^5 could be obtained.

4.Conclusion

We have presented the electrical characteristics of pentacene organic thin film transistors fabricated on flexible polyethersulfone (PES) film through a four-level shadow mask process. The alignment technique by using shadow-mask was used to form source/drain since it was expected to provide a low cost process and it is possible to one-step process from patterning to passivation without breaking vacuum in the chamber.

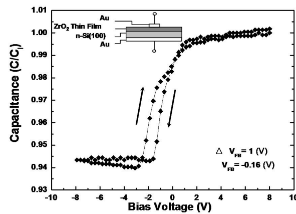
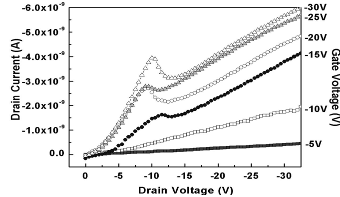
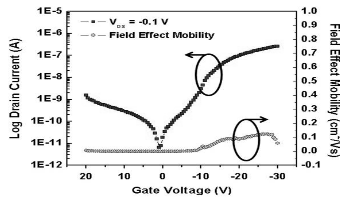


Figure1. High frequency (1 MHz) capacitance (C-V) characteristics of the dielectric layer (ZrO2) deposited on a heavily doped n-type silicon substrate.



(a)



(b)

Figure2. Electrical properties of shadow-mask processed TFT in the absence of OTMS treatment on gate insulator. (a) Electrical characteristics of drain current (ID) vs voltage (VD) at various gate voltages (VG) and (b) Electrical characteristics of ID vs VG and field effect mobility at drain voltages (VD) of 0.1 V.

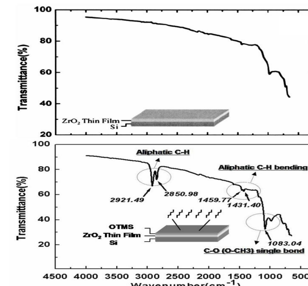
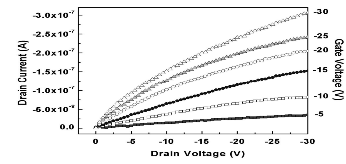
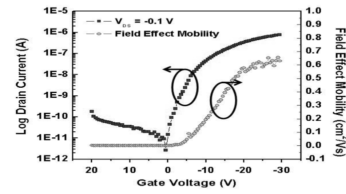


Figure 3. Infra-red spectra of the ZrO2-OTMS deposition. Sample was prepared by deposition of ZrO2 on the silicon wafer followed by surface treatment of the OTMS.



(a)



(b)

Figure 4. Electrical properties of shadow-mask processed TFT in the presence of OTMS treatment on gate insulator. (a) Electrical characteristics of drain current (ID) vs voltage (VD) at various gate voltages (VG) and (b) Electrical characteristics of ID vs VG and field effect mobility at drain voltages (VD) of 0.1 V.

Reference

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