LC VCO using dual metal inductor in 0.18 μm mixed signal CMOS process

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Abstract - This paper presents the design and fabrication of a LC voltage-controlled oscillator (VCO) using 1-poly 6-metal mixed signal CMOS process. To obtain the high-quality factor inductor in LC resonator, patterned-ground shields (PGS) is placed under the symmetric inductor to reduce the effect from image current of resistive Si substrate. Moreover, due to the incapability of using thick top metal layer of which the thickness is over 2 μm, as used in many RF CMOS process, the structure of dual-metal layer in which we make electrically short circuit between the top metal and the next metal below it by a great number of via materials along the metal traces is adopted. The circuit operated from 2.63 GHz to 3.09 GHz tuned by accumulation-mode MOS varactor. The corresponding tuning range was 460 MHz. The measured phase noise was -115 dBc/Hz @ 1MHz offset at 2.63 GHz carrier frequency and the current consumption and the corresponding power consumption were about 2.6 mA and 4.68 mW respectively.

Introduction

Integrated LC voltage-controlled oscillators (VCOs) are common functional blocks in modern high frequency communication systems and are used as local oscillator to up- and downconverter signals. In designing an integrated CMOS LC VCO, phase noise, power consumption, chip area, manufacturing cost are important issues. Above all, phase noise is the most important characteristic because VCO noise enters directly into up- down converter, and this can affect the noise performance of total communication system. Moreover due to the ever-increasinng demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators.

The key to the design of a low phase-noise oscillator is a high quality inductor as it has been shown for several studies. And the quality factor of the inductor will be limited by the series resistance of the metal traces. In case of using foundries providing RF CMOS process, designers can implement inductors using thick metal and this enables oscillators to have excellent noise performance.

But RF CMOS process requires higher cost than mixed signal CMOS process that is for baseband analog and digital applications. Moreover conventional mixed signal CMOS process is still easier to access for ordinary analog circuit designers.

Design and Fabrication

Schematic of complementary LC VCO and its layout were shown in Fig. 1 and Fig. 2 respectively. It is designed using the methodolgy of finding the optimum inductance of resonator, the varactor size for desired tuning frequency and the active device size for low power consumption. As shown in Fig. 2, designed LC VCO was fabricated using mixed signal 1-poly 6-metal mixed signal CMOS process. To overcome disadvantage due to using thin metal of which the thickness is one fourth of RF-aimed thick metal, we made coil thicker by connecting the metal 6 and metal 5 by a great number of via 5 materials. Consequently, this led to the decrease of series resistance and increase of VCO noise performance.

The area of VCO circuit including pads is about 0.51 x 0.62 mm^2. To suppress the substrate loss in symmetric inductor, poly PGS was placed and the grounded M1 shields were used underneath MIM capacitors and RF interconnects.

Experimental Results

In the measurement, supply voltage of 1.8 V was applied and tuning voltage was varied from 0 V to 1.8 V. Total current flowing into the bias circuit was 2.6 mA. Core circuit consumed 1.3 mA. Accordingly, power consumption was measured to be 4.68 mW. Fig. 3 shows the measured tuning curve. The oscillator operated from 2.63 GHz to 3.09 GHz and corresponding tuning range was 460 MHz. Fig. 4 shows the measured frequency spectrum at V_c = 1.8 V. The measured phase noise versus offset frequency at V_c = 1.8 V is shown in Fig. 5. The measured phase noise was -115 dBc/Hz @ 1 MHz at V_c = 1.8 V. It is obviously shown from this work that good phase noise characteristic can be achieved without using thick metal provided by RF CMOS process.

A widely used figure of merit (FOM) for the VCO is defined as follows,

$$\text{FOM} = L\{f_{offset}\} - 20\log\left(\frac{f_0}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1\text{ mW}}\right)$$

From above equation, FOM of the fabricated VCO can be calculated to be -176.7 dB.

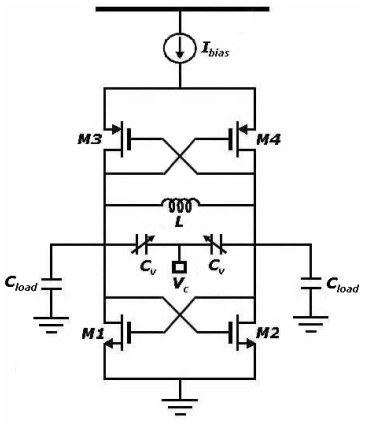

Fig. 1. Complementary LC VCO schematic.

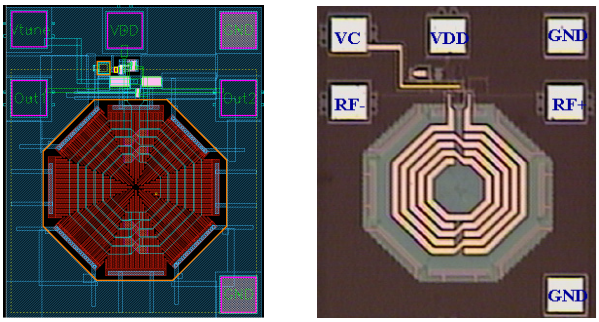

Fig. 2. LC VCO layout and chip photograph.

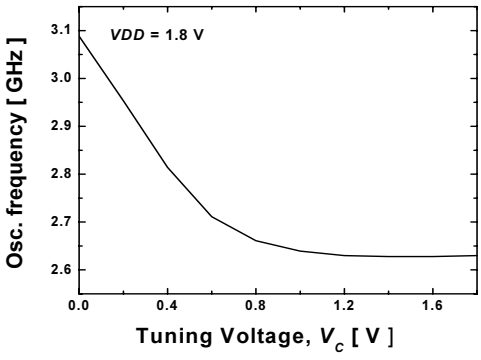

Fig. 3. Measured frequency tuning curve.

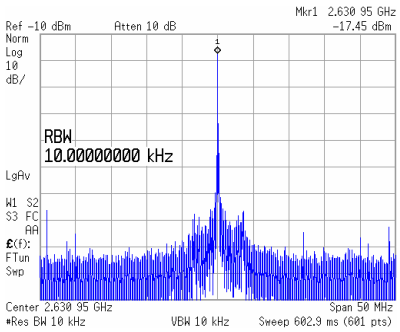

Fig. 4. Measured frequency spectrum for V_c = 1.8 V.

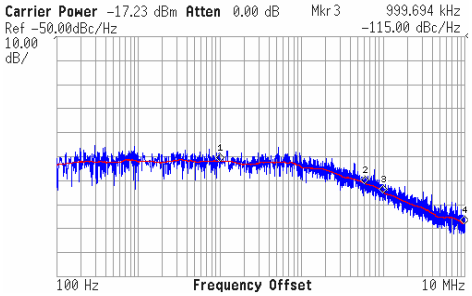

Fig. 5. Measured phase noise for V_c = 1.8 V.

Conclusions

An integrated LC VCO was fabricated using conventional mixed signal CMOS process. The VCO operated from 2.63 GHz to 3.09 GHz and quite low phase noise of -115 dBc/Hz at 1 MHz offset was achieved. By adopting dual metal layer inductor, it was shown that the phase noise of LC VCO can be improved even in thin-metal based mixed signal CMOS process.

Acknowledgement

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References

[1] M. Hershenson, A. Hajimiri, S. S. Mohan, S, P. Boyd, and T. H. Lee. "Design and Optimization of LC Oscillators," *IEEE/ACM Int. Conf*, *Computer Aided Design*, pp. 65-69, Nov.1999.
[2] Ali Hajimiri and T. H. Lee "Design Issues in CMOS Differential LC Oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717-724, May 1999.
[3] D. Ham and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896-909, June. 2001.
[4] S. Song and H. Shin, "A New RF Model for the Accumulation-Mode MOS Varactor," *IEEE MTT-S* , June 2003.
[5] J. Gil, S. Song, H. Lee, and H. Shin "A -119.2 dBc/Hz at 1 MHz, 1.5 mW, Fully Integrated, 2.5-GHz, CMOS VCO Using Helical Inductors," *IEEE Microwave and Components Letters,* vol. 13, no. 11, Nov. 2003.