A 915-MHz RF CMOS Low Power High Gain Amplifier using Q-Enhancement Technique for WPAN

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Abstract

In this paper low power high gain amplifier is suitable for application in low power systems was designed and fabricated. The amplifier used both subthreshold bias for low power and positive feedback Q-enhancement technique for high gain. The amplifier used TSCM 0.18μm RF CMOS technology measures a power gain of 32.3dB, a quality factor of 366 and a power consumption of 3mW in a supply voltage of 1.8V.

I. INTRODUCTION

Recently, low power consumption has been important issue in the wireless telecommunication system. Especially, that is the most important performance in the low power wireless systems as WPAN [1]. Accordingly, the key parameter in the success of future wireless systems will be a long battery life. In other words, developers of wireless system want to realize a low power circuit.

In this paper a very low power high gain amplifier was implemented using CMOS technology in 915MHz band which has the ability to incorporate cost-effective VLSI designs.

II. CIRCUIT DESIGN

A. Q-Enhancement Circuit

The Q-enhancement circuit is similar to oscillator, as shown in Figure 1. The basic function of the Q-enhancement circuit is to add a negative resistance to the LC resonator to compensate the losses. This function is realized by cross coupled transistor shown Figure 1. When negative transconductance of the circuit is generated, the resulting Q is :

$$Q = \frac{\omega_0 C}{g_0 - g_{mn}} \quad (1)$$

Where the negative transconductance of cross coupled transistor is g_{mn}, the equivalent parallel losses in the LC resonator circuit are denoted by g_0. If setting g_{mn} close to g_0, the Q of the enhancement circuit can be set high. However, if g_{mn} is set larger than g_0, the enhancement circuit will be made an oscillation [2-4]. C is the capacitance of the LC resonator circuit and ω_0 is the center frequency of Q-enhancement circuit.

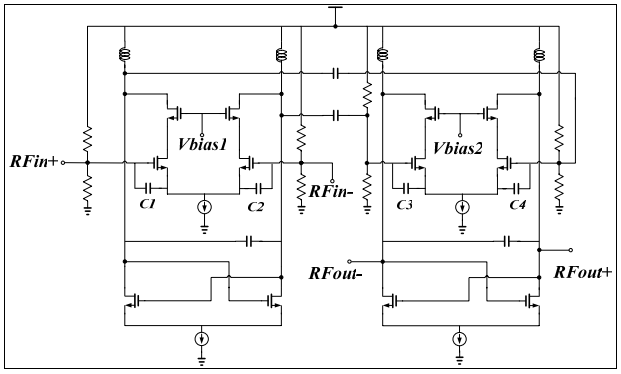

Fig. 1 Low power high gain amplifier with Q-enhancement circuit

B. Low Power Amplifier

The designed low power high gain amplifier consists of Q-enhancement circuit and amplitude part.

The amplitude part was operated in the weak inversion. The circuit of weak inversion region is possible to design extremely low power CMOS circuit because subthreshold biasing enables the most DC gain for the least amount of current, as evidenced by the high g_m/I_D ratio in this region. Generally for a given bias current, the available transconductance g_m may be several times higher than in strong inversion [5]. The current of the weak inversion region is given by

$$I_{SUB} = \frac{W}{L} \cdot I_0 \cdot \exp\left(\frac{qV_{GS}}{nKT}\right) \quad (2)$$

Where W and L are width and length of transistor, n is subthreshold slope factor, I_0 may be understood as s technology dependent parameter [6].

The designed amplifier was biased in a subthreshold area for low power. Parallel capacitors(C1~C4) are capacitance to help matching circuit, and load inductors, inductance of the resonator circuit were used by off chip element.

III. MEASURED RESULTS

To obtain accurate results, length of bond wire, ESD(Electro Static Discharge) circuit and parasitic elements were considered during the simulation. Moreover, passive components of off chip matching circuits were used scattering parameters.

Figure 2 shows the microphotograph of amplifier with Q-enhancement circuit. The low power high gain amplifier was implemented in 0.18μm 6-metal RF CMOS process. Core size of amplifier is 570μm × 290μm except ESD circuit and PAD.

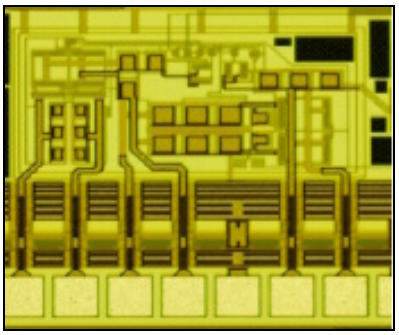

Fig. 2 Die photograph of the amplifier

The implemented amplifier was measured power gain of 32.3dB and current of 1.67mA at 915MHz. And the quality factor was found to be 366. The frequency tuning range of amplifier is 10MHz. The reason why tuning range is narrow, is to fine tuning. However if large variable capacitor was used, amplifier provided a high gain in a wide range.

Figure 3 shows the power gain and frequency tuning range of the amplifier.

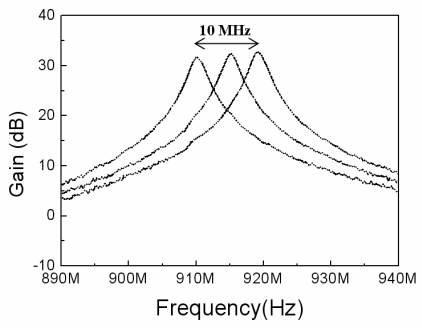

Fig. 3 Frequency response of the amplifier tuned at different frequency.

The center frequency of the Q-enhancement circuit is set a 915MHz. The performances of the low power high gain amplifier are summarized in Table I.

TABLE I
Summary of high gain amplifier performance

Technology	TSMC 0.18um RF CMOS
Area	570μm X 290μm
Supply voltage	1.8 V
Center Frequency	915 MHz
Power Gain	32.3 dB
Quality Factor	366
Current amplitude	1.57 mA
Q-enhancement	100 μA
Power Consumption	3 mW

IV. CONCLUSION

In this research, we demonstrated a low power high gain amplifier with Q-enhancement circuit at 915MHz. The amplifier has been designed using 0.18μm CMOS technology. A high quality factor of 366 was achievable through introducing a negative resistance by means of positive feedback. And a high gain of 32.3dB was obtained at a low power consumption of 3mW. This amplifier can be applicable to various systems if that can be tuned a frequency by control the capacitance of variable capacitor in resonator or by changing the center frequency of Q-enhancement circuit.

V. REFRENCE

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