A Dual-Band CMOS Low-Noise Amplifier

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Abstracts – This paper presents a switch type 2.4/5.8 GHz dual band low-noise amplifier, designed with 0.13 μm RF CMOS technology. Using MOS switch allows the LNA to have two different input transconductance and output capacitance modes. Given supply voltage of 1.2 V, the simulation exhibits gains of 8.1 dB and 17.1 dB, noise figures of 3.1 dB and 2.57 dB and power consumptions of 13.0 mW and 10.2 mW at 2.4 GHz and 5.8 GHz, respectively.

1. Introduction

With the growing demand for the wireless application products, the low-cost and high integration have become the essential design targets for the communication ICs. Multi-standard radio frequency transceivers are predicted to play a critical role in wireless communication. Two ways can approach the goal: wideband and multiband structure. Wideband structure is sensitive to out-of-band signals due to non-linearity of transistors. As the several bands are close by, wideband architectures are desirable in standard receivers for utilization of the available bandwidth. However, multiband structure results in better performance for some useful narrow bands.

2. Results and Discussion

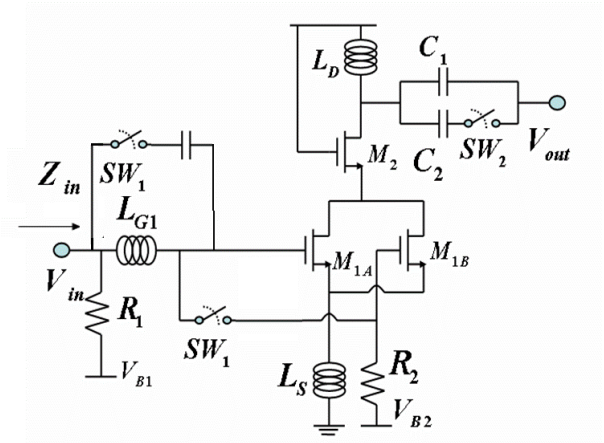


Fig 1. Complete Schematic of the Dual-band LNA

A switch-type circuit topology is used. Figure 1 shows the complete schematic of the proposed 2.4/5.8 dual-band LNA. The LNA has source degenerated cascade amplifier and switched transistors for band selection. There are two modes depending on status of switch transistors, SW_1 and SW_2.

When the LNA operates at 5.8 GHz, SW_1 and SW_2 are open. Bias of M_{1B} gate is set to be V_{B2}, which is slightly lower than the threshold voltage of M_{1B} in this case. Since M_{1B} is off, a conventional source-degenerated LNA design is possible. The input impedance of the LNA at 5.8 GHz can explicitly be shown as

$$Z_{in,5.8} \approx \frac{g_{m1A}L_S}{C_{gs1A}} + j\omega_{5.8}(L_S + L_{G1}) + \frac{1}{j\omega_{5.8}C_{gs1A}} \quad (1)$$

g_{m1A} and C_{gs1A} are the transconductance and the gate capacitance of M_{1A}. The component size of L_S, g_{m1A} and C_{gs1A} are decided to produce real 50 Ω. And then, the size of L_{G1} is chosen to make the imaginary term zero at 5.8 GHz. As we increase the width of M_{1A}, g_{m1A} goes up resulting in gain increment at 5.8 GHz. Negative imaginary term of Z_{in} will be reduced because C_{gs1A} also rises up. Thus, L_{G1} for compensating imaginary part becomes smaller. Based on the fact that growing up L_{G1} size goes with increased resistance in L_{G1}, which is critical noise source in the input stage, this trend is also desirable for noise performance. Even though we can improve the gain and noise performance by increasing number of fingers in transistor, we should note that the power consumption of circuit rise up dramatically. In deciding device size of M_{1A}, trade-off between gain, noise and power should be considered.

When the LNA operates at 2.4 GHz, SW_1 and SW_2 are closed. Gate bias of M1A, which is equal to M2B, is

$$\frac{R_2V_{B1} + R_1V_{B2}}{R_1 + R_2}$$

decided by the voltage divider R_1 and R_2. This value will be smaller than V_{B1}, for V_{B1} is larger than V_{B2}. To increase this value, it is advisable to increase the R_2/R_1 ratio.

The resulting input impedance without L_{G2} at 2.4 GHz can be expressed as

$$Z_{in,3.0} \approx \frac{(g_{m1A} + g_{m1B})L_S}{C_{gs1A} + C_{gs1B}}$$

$$+ j\omega_{2.4}L_S + j\omega_{2.4}L_{G1} // \frac{1}{j\omega_{2.4}C_g} + \frac{1}{j\omega_{2.4}(C_{gs1A} + C_{gs1B})}$$

……(2)

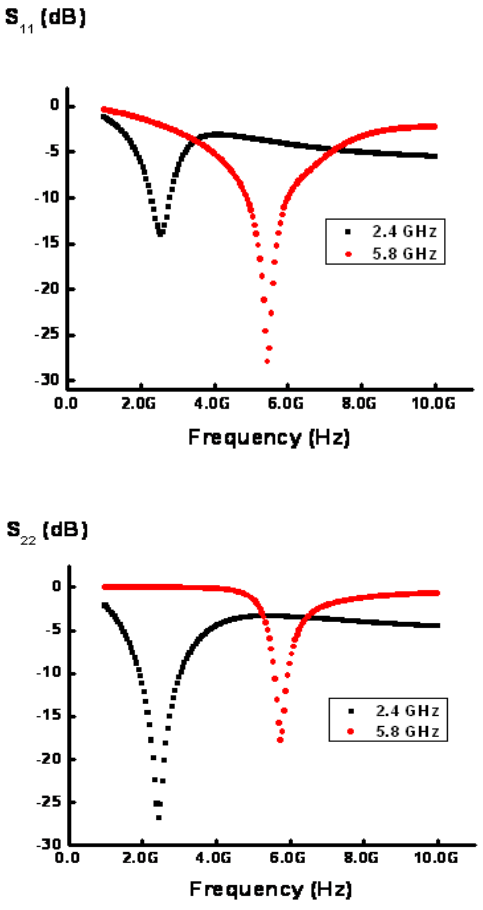
where g_{m1B} and C_{gs1B} are the transconductance and the gate capacitance of M_{1B}. L_{G1}, L_S and C_{gs1A} is already

decided previously when designing the LNA to operate optimally at 5.8 GHz. Using LC tank in a input stage allows us to realize a large inductance. Since the third term of (2) have a large positive imaginary near resonance frequency, the low operating frequency of the circuit can go down further.

In input switch SW_1, there are two non-ideal characteristics to be considered at both on and off states. Even when the transistor is off, this MOS switch is connected to signal ground with capacitors. These capacitors become larger and move input matching frequency as we increase number of finger. When a switch is on, on-resistance between the source and the drain appears and forms noise source at input stage. The choice of large transistor size for SW_1 will reduce noise performance degradation. The size of SW_1 is optimized to minimize parasitic capacitance in off-state and noise performance degradation in on-state.

Same consideration applies to the size of output MOS switch SW_2. When the circuit operates at 2.4 GHz, we can see that the resonance frequency moves down to

$$\frac{1}{2\pi\sqrt{L_D(C_1+C_2)}} \quad \text{from} \quad \frac{1}{2\pi\sqrt{L_D C_1}} \quad @5.8\ \text{GHz}$$



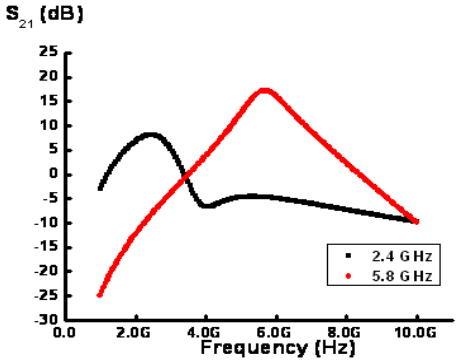


Fig 2. S-parameter Results of the Dual-band LNA

The simulation was performed by using standard 0.13 μm CMOS process. The simulation results are displayed in Fig 2. and Table I below.

Frequency	2.4 GHz	5.8 GHz
Power Dissipation	13.0 mW	10.2 mW
S_{21}	8.1 dB	17.1 dB
S_{12}	-50.3 dB	-32.8 dB
S_{11}	-12.3 dB	-12.8 dB
S_{22}	-25.2 dB	-16.8 dB
Noise Figure	3.1 dB	2.57 dB
Supply voltage	1.2 V	

Table. 1. The Performance Summary of the Proposed LNA.

3. Conclusions

In this paper, a switch type dual-band LNA design techniques have been presented. The circuit has two modes depending on the states of MOS switch SW_1 and SW_2. The input matching is achieved by switching the finger number and the bias voltage of the input transistor, while the output matching is accomplished by a switched capacitor. Simulation results show that the proposed input and output matching networks work well.

4. Acknowledgement

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