

Design of Down-conversion Double Balanced Mixer using InGaP/GaAs HBT Technology

Won-Jun Choi, Se-Hwan Kim, Jung Heo, Bhanu Shrestha,

*Sang-Hoon Cheon and Nam-Young Kim

RFIC Research and Education Center, Department of Electronic Engineering,

Kwangwoon University, Seoul, 139-701, Korea

E- mail: honest16@hanmail.net

*Knowledge*on Inc.

513-7 Euyang-dong, Iksan 570-210, Korea

Abstract

In this paper, the double balanced mixer (DBM) for adaptive feedback-interference cancellation system (AF-ICS) is developed using InGaP/GaAs heterojunction bipolar transistor (HBT) technology. This circuit is designed with internal bias supply, common collector output buffer for impedance reduction and degeneration capacitor to improve linearity within a total area of $875 \times 775 \mu\text{m}^2$. Simulation result shows the mixer achieves a conversion gain of 3.1 dB, a third-order input intercept point (IIP₃) of 12.77 dBm, a third-order output intercept point (OIP₃) of 15.87 dBm.

I. Introduction

Modern wireless communication system is getting better and better day by day. A number of techniques are invented for enhanced system. The adaptive feedback-interference cancellation system (AF-ICS) is one of those techniques. It is suggested in order to cancel the feedback signal in the wireless communication system and maintains the maximum output power of the power amplifier by the reduction of time-varying feedback signal. The feedback signal becomes the source of interference and the performance of the receiver system is decreased by the feedback signal. So, this feedback signal should be cancelled in order to maintain the system performance. Fig. 1. shows the block diagram of AF-ICS [1].

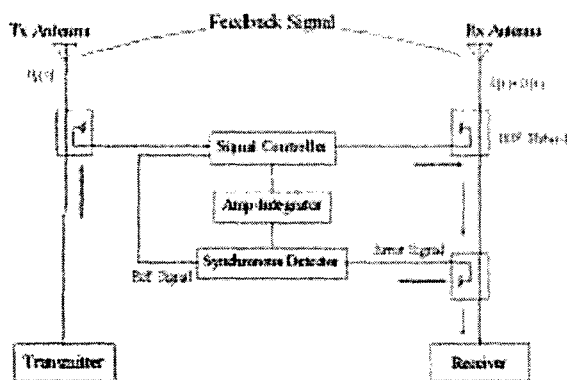


Fig. 1. The general block diagram of the adaptive feedback interference cancellation system (AF-ICS)

For this system, the mixer should be designed by considering the several parameters like linearity, conversion gain, input/output ports leakage isolation, intermodulation distortion (IMD) etc. Linearity is one of the most important parameters. This system works well under the guaranteed linearity. Therefore, this mixer is designed in such a way that, the degeneration capacitor with common collector output buffer is used to get high third-order output intercept point (OIP₃) and low current of buffer for AF-ICS is designed using InGaP/GaAs HBT high linearity process of Knowledge*on Inc.. It also has a very good isolation performance.

II. InGaP/GaAs HBT MMIC Process

The heterojunction bipolar transistor (HBT) offers a more efficient approach in various front-end signal-processing functions than advanced Si homojunction bipolar transistors and III-V compound field-effect transistor (MESFET and HEMT) technology. Although the GaAs HBT has higher white noise than III-V FETs, advantages have greater speeds with relaxed lithographic dimension, higher transconductance, higher current per effective chip, better device matching, lower output conductance, and reduced trapping effects accompanied by low 1/f and phase noise. As compared to advanced Si BJT technologies, the GaAs HBT is limited in integration complexity, but offers advantages of higher speeds with relaxed lithographic dimensions, lower output conductance, effectively no parasitic substrate capacitance, and greater radiation hardness [2]. The scanning electronic microscope (SEM) picture of InGaP/GaAs HBT used in this design is shown in Fig. 2., which has 2 finger, emitter width $2 \mu\text{m}$, emitter length $20 \mu\text{m}$, high linearity (HL_F2x2x20).