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Fabrication of self-aligned thin film transistor with an ultra low temperature polycrystalline silicon process on stainless steel foil substrate

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We have fabricated self-aligned p-channel thin film transistors (TFTs) with an ultra low temperature polycrystalline silicon process on stainless steel foil substrates. Various processing issues such as substrate planarization [1], laser crystallization of amorphous Si films[2] and formation of high quality gate dieletrics using a plasma-enhanced atomic layer deposition[3] have been addressed. In particular a practical approach for realizing micron size Si grains on a SiO_2 buffer has been discussed in detail. The fabricated device exhibited a field effect mobility of 95 cm^2/Vs, a threshold voltage (V_t) of -3 V and a sub-threshold swing(S-S) of 0.5 V/dec.

[참고문헌]

1. Jaehyun Moon et al., IEEE Electron Device Lett., submitted.
2. Yong-Hae Kim et al., IEEE Electron Device Lett. **25**, 550 (2004).
2. Sun Jin Yun et al., Electrochem. Solid-state Lett, **7**, C13 (2004).