

Parallel Performance Assessment of Moving Body Overset Grid Application on PC cluster

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ABSTRACT

The multi-block overset grid method is a powerful technique for high-fidelity computational fluid dynamics(CFD) simulations about complex aerospace configurations[1]. Furthermore, it allows the calculation of moving-body with relative motions, such as applications in the analysis of store separation and many other areas. However, a communication between overlapping grids must be re-established in every time step as the sub-grid is moved. This process of establishing communication between overlapping grids involved in hole cutting and domain connection has been referred to as "grid assembly"[2].

The parallel implementations and performance assessments of the well known chimera codes, Beggar[2] and DCF3D[3] have been accomplished on vendor's machines, such as SGI, IBM, and Cray. In this research, a structured multi-block grid assembly is parallelized by using a static load balancing tied to flow solver based on a grid size of decomposed domain. The parallel algorithm is modified for a distributed memory system typically PC cluster, which has some advantages typically low cost & high performance and therefore is widely used in nowadays.

A message passing programming model based on the MPI library is implemented using the Single Program Multiple Data(SPMD) paradigm. A coarse-grained communication is optimized with the minimized memory allocation and communication load because the parallel grid assembly can access the decomposed geometry data within other processors by only message passing in the distributed memory system such as the PC cluster.

This parallel grid assembly and flow solver(KFLOW[4]) are tested on the store separation problem from the Eglin wing and pylon configuration[5] in inviscid flow field, and the parallel performance assessment is presented. The numerical fluxes at cell interface are constructed Roe's flux difference splitting method and MUSCL(Monotone Upwind Scheme for Conservation Law) scheme. For the time integration, diagonalized ADI method is used with 2nd-order dual time stepping algorithm.

Figure 1 is the flow chart of parallel grid assembly. The coarse-grained communication between each processor are inserted in construction of hole-map, hole cutting and donor searching routine. Linux PC cluster with P4-2.6GHz CPU in each node and linked by 100Mbps Ethernet network is used. Serial and parallel computing with 15 and 30 nodes are performed.

Figure 2 shows the constructed overlap grids and the pressure contour at initial position and

initial IGBPs(Inter-Grid Boundary Points) are 126,534. Figure 3 is the simulated CG location and attitude of store and the experimental data[5]. Table 1 and 2 show parallel performance of each routine for the grid assembly, the domain connection(total interpolation work time in every time step) and the flow solving. Total speed up ratio in case of using 30 processors is 17.58. This is about 59% of a ideal parallel performance. Most time consuming parts of grid assembly and domain connection routine are data communication through network. A higher performance network system, for example the Myrinet, can reduce communication time in these routines. However, a larger number of processors is better than the expensive network system because the limitation of static load balancing tied to flow solver in grid assembly still remains and flow solver routine is 60% of total work.

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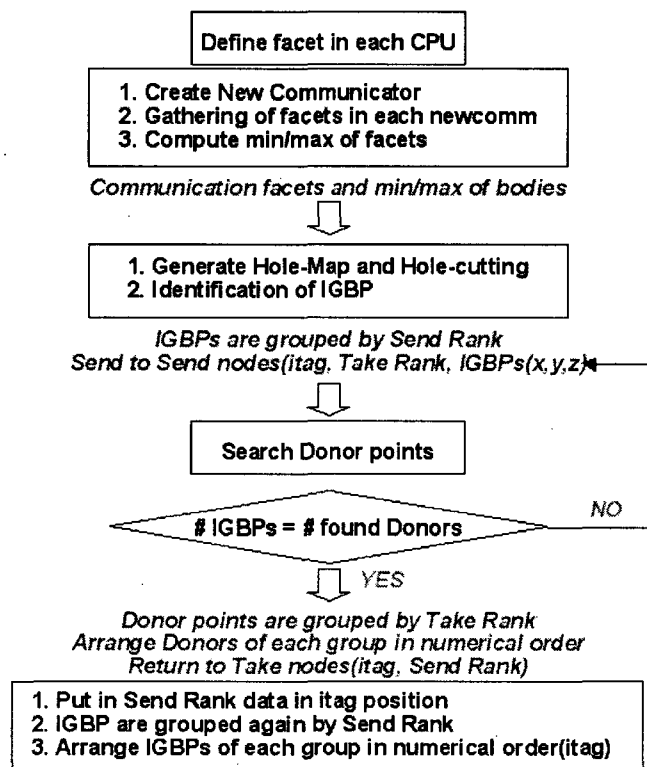


Fig. 1 Process of grid assembly

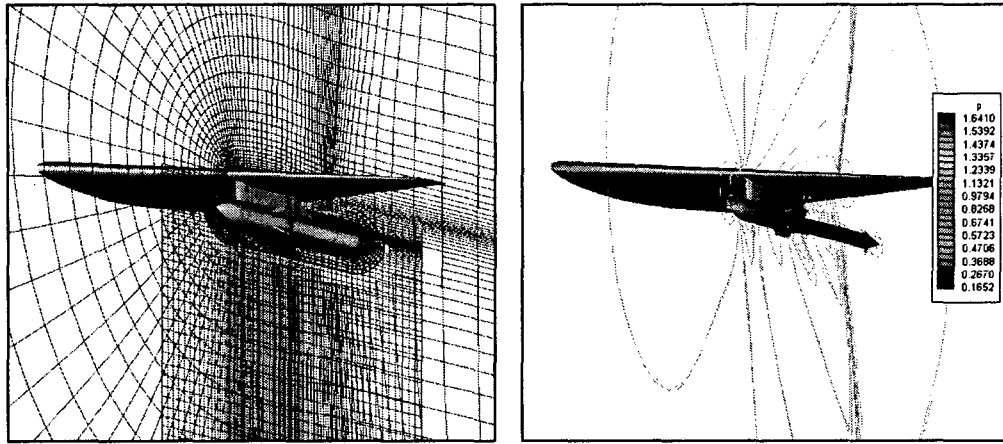


Fig. 2 Overset grids and pressure contour at the initial condition

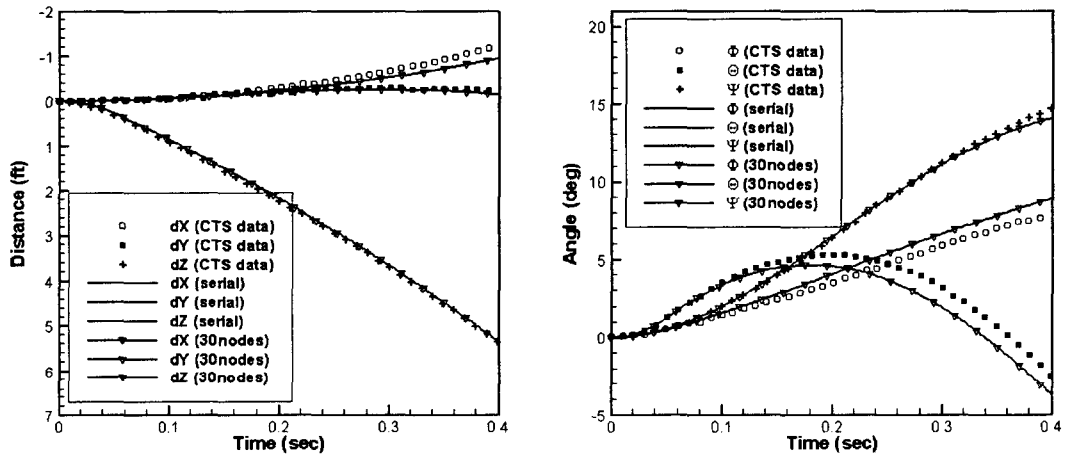


Fig. 3 Store trajectory (dt=0.00195 sec)

Proc.	Grid assembly		Domain connection		Flow solver		Total	
	W time	CPU time	W time	CPU time	W time	CPU time	W time	CPU time
Serial	26754.2	1863.4	3111.9	1587.4	375325.8	315182.8	410459.3	342534.7
15	4781.7	972.2	6231.8	119.5	41524.7	21913.9	53221.1	23634.7
30	4069.5	756.6	4871.3	46.5	14126.5	9213.6	23346.3	10246.8

Table 1 Parallel performance(wall clock time and CPU time)

Proc.	Grid assembly	Domain connection	Flow solver	Total
15	5.596	0.499	9.039	7.712
30	6.574	0.639	26.569	17.581

Table 2 Speed up of each module in CPU time(fraction of wall clock time)