Design And Implementation of a Novel Sustain Driver for Plasma Display Panel

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ABSTRACT

Over the years, plasma display panel (PDP) manufacturers have impressed the flat panel display industry with yet another new product essentially having the merits of a larger screen size. Since larger size implies higher power ratings, voltage/current ratings of the power devices used have become a rising concern. Another important concern is the brightness of PDP, one way of increasing which is by operating the PDP at higher frequencies. In order to address the above issues, a transformer coupled sustain-driver for AC-PDP is proposed. During the transition time, the two windings of the transformer greatly boost up the displacement current flowing through the panel capacitance and hence enable a fast inversion of the voltage polarity with practical values of resonant inductance. In the proposed topology, the resonant inductance can be increased by a factor of $(n+1)^2$ as compared to prior approaches. Increased inductance results in lower current stresses. Moreover, high frequency operation is possible by using higher value of n (turn ratio of the transformer). The operational principle and design procedure of the proposed circuit are presented with theoretical analysis. The validity of the proposed sustain driver is established through simulation and experimental results using a 42-in PDP

1. INTRODUCTION

In the area of rapidly evolving flat panel display technology, the plasma display panel (PDP) stands out as a promising candidate with assets including large screen size, wide viewing angle, thinness, and high contrast ratio[1]. Various types of sustain drivers, which do away with the CV^2 energy loss of switching devices by adopting the L-C resonant technique, have been proposed earlier as in[2-5]. However, these circuits have high current stress during the resonant period.

In this paper, a novel topology is proposed for operating the PDP panel with reduced resonant current stresses. Using a transformer (with n as the secondary to primary turns ratio) in parallel with the panel capacitance, the required resonant inductance can now be increased by a factor of $(n+1)^2$ and consequently the resonant current is reduced significantly as compared to the prior approach [2]. The operational principle, mode analysis and design procedure of the proposed circuit are explained with theoretical reasoning in subsequent sections. The validity of the proposed sustain driver is established through simulation and experimental results using a 42-in PDP.

2. PROPOSED SUSTAIN DRIVER

2.1 Circuit Configuration

Figure 1 shows the configuration of the proposed transformer based energy recovery sustain driver. S_1, S_2, S_3 and S_4 are the sustain switches; S_5, S_6, D_5, D_6 & S_7, S_8, D_7, D_8 constitute two separate bidirectional switch networks; XR is a transformer with a 1:n primary to secondary winding turns ratio and L_R is a resonant inductor connected in series with the secondary side of XR. The clamping diodes (D_1, D_2, D_3 and D_4) have been shown here for technical completeness but will not be discussed further to avoid complexity.

2.2 Mode Analysis

Figure 2 shows the operational waveforms of the proposed sustain driver. For simplicity in understanding the key idea of the proposed scheme, switches and diodes are assumed to be ideal. Another key assumption here is that the magnetizing inductance of the transformer is much greater than the resonant inductance. Since the operation of the two half cycles is symmetric, mode analysis is performed only for the first half cycle. The detailed mode by mode analysis is as follows.

Mode 1($t_0 \le t \le t_1$): Just before t_0, switches S_2 and S_3 are in the on state and all the other switches are off. The voltage across the panel is maintained at the sustain voltage level ($-V_S$). At t_0, switches S_6 and S_8 are turned on. The current

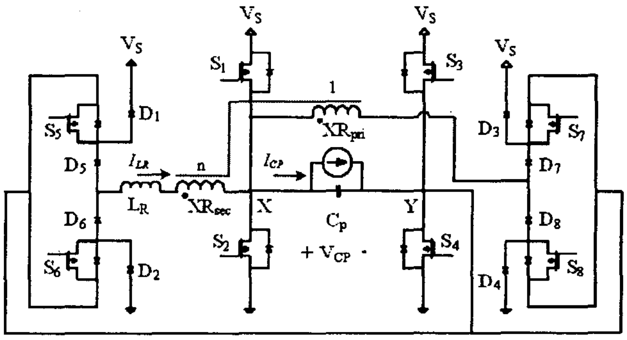

Fig.1 Proposed Topology

in the resonant inductor (L_R) builds up linearly as shown in (1). This build up current is necessary to make up for the energy losses in the parasitics and non-idealities such as diode voltage drops, switch-on resistance, etc during the transition period (Mode 2) and enable ZVS operation of the main full-bridge switches

$$L_R \frac{di_{LR}}{dt} = (n+1)V_S \tag{1}$$

At t_1, the build up current is

$$I_0 = (n+1)\frac{V_S \delta t}{L_R}, \; where \; \delta t = t_1 - t_0 \tag{2}$$

Mode 2($t_1 \le t \le t_2$): At t_1, switches S_2 and S_3 are turned off. The equivalent circuit during this mode is shown in Figure 3. The differential equation for this mode is as shown in (3).

$$L_R C_p \frac{d^2x}{dt^2} + (n+1)^2 x = 0 \tag{3}$$

In the equation above, x is the system state - either the resonant inductor current (i_{LR}) or the panel voltage (v_{CP}). For initial conditions (i_{LR} = I_0, , v_{CP} = $-V_s$), the solution of the differential equation is as follows.

$$v_{CP}(t) = -V_S \cos(n+1)w_0 t + I_0 \sqrt{\frac{L_R}{C_P}} \sin(n+1)w_0 t,$$

$$\omega_0 = \frac{1}{\sqrt{L_R C_p}} \tag{4}$$

Substituting (2) into the above equation yields the design equation,

$$v_{CP}(t) = -V_S \cos(n+1)w_0 t + (n+1)V_S.\delta t.w_0 \sin(n+1)w_0 t \tag{5}$$

As shown in (5), the natural frequency of the self oscillatory circuit during this mode is $(n+1)\omega_0$. This implies that the resonance is (n+1) times faster here than a conventional series resonance for the same value of the resonant inductor. In other words, when keeping the same transition time, the inductance can be increased by a factor of $(n+1)^2$ which would result in a lower current stress both in the resonant inductor as well as the auxiliary switches and diodes.

Mode 3($t_2 \le t \le t_3$): At t_2, switches S_1 and S_4 are turned on with ZVS. Discharge current for the panel is supplied by the source. The current remaining in the inductor decreases linearly as shown in (6).

$$L_R \frac{di_{LR}}{dt} = -(n+1)V_S \tag{6}$$

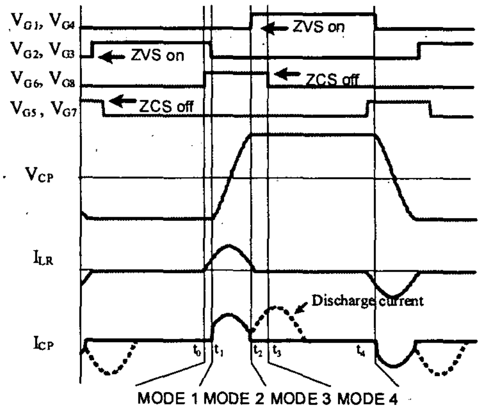

Fig. 2 Mode Analysis

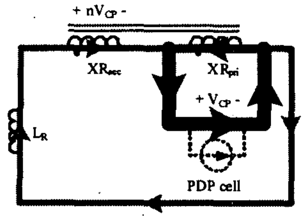

Fig. 3 Equivalent circuit during Mode 1 and Mode 4

At t_3, the current flowing through the inductor is zero. Switches S_6 and S_8 are turned off with ZCS.

Mode 4($t_3 \le t \le t_4$): During this mode, the voltage across the panel is V_S. The discharge current continues to flow through the sustain switches. The resonant inductor and the transformer do not carry any current during this mode and hence there are no circulating losses.

The remaining half cycle is similar to the analysis done above.

3. DESIGN

Here, the design variables are n (turns ratio of the transformer), L_R and δt (current build-up time). They can be determined from (5).

Since the above equation cannot be expressed as an explicit function of the design variables, they can be calculated using an iterative method. However to avoid any mathematical complexity and to put across the key concept of the proposed topology, δt is set to zero. This makes the equation simple as shown in (7).

$$v_{CP}(t) = -V_S \cos(n+1)w_0 t \tag{7}$$

By choosing an appropriate transition time, L_R can be determined as a function of n, panel capacitance (nearly 80 nF for 42-in PDP) and the transition time.

4. EXPERIMENTAL RESULTS

The validity of the proposed sustain-driver is established through experimental results using a 42-in PDP. Using the design equations discussed earlier and fixing the transition time as 700 ns the design variables are determined to be L_R = 2.3 uH, n = 1 and δt = 0 us. The magnetizing inductance, L_M, is designed as 30 uH to satisfy the assumption ($L_R << L_M$). The sustain voltage across the panel and the resonant inductor current are shown in Figure 4. Here, the inductor current goes a bit beyond zero and freewheels because of the parasitic capacitance of the energy recovery (auxiliary) switch and clamping diode.

For comparison, the waveforms using commercially used topology[2] is also shown in Figure 5.

In order to get some idea of the efficiency, the current consumption curves using different number of sustain pulses for both the proposed and the conventional scheme is plotted in Figure 6.

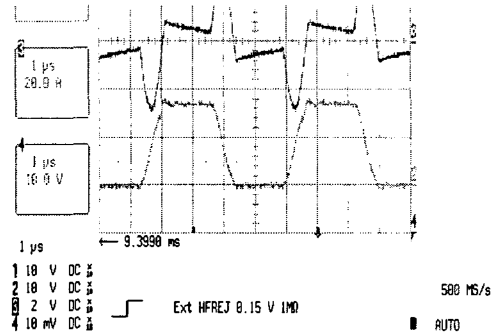

Fig. 4 Key waveforms of the proposed topology VX (Blue), VY (Green), ILR (Red)

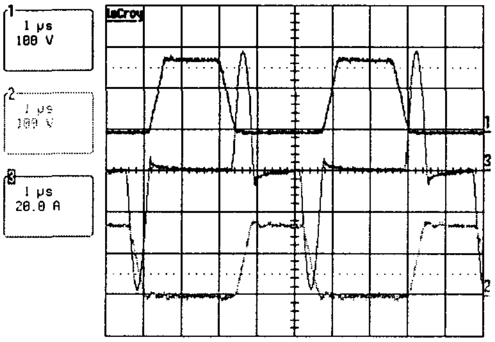

Fig. 5 Key waveforms of the Weber topology VX (Blue), VY (Green), ILR (Red)

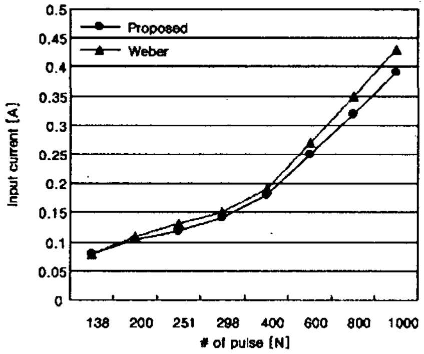

Fig. 6 Current Consumption vs. Number of Sustain Pulses

5. DISCUSSIONS

The experimental results shown in the previous section confirm the high current stresses of auxiliary switches and diodes in the conventional topology as compared to the proposed one. In fact, the current shown in Figure 5 is sensed only on the Y-Board. A similar current flows on the X-Board. So, basically for a transition of the panel voltage (V_{XY}) from $-V_S$ to $+V_S$, the current consumption is nearly doubled in the Weber topology.

Moreover, another point worth noting is the sensitivity of the resonant inductor value. While attempting to achieve a shorter transition time (< 0.7 us), the inductor values in the proposed configuration are on the order of uH, while those in Weber's topology are on the order of nH, thus posing practical difficulties such as controllability of the resonant inductor value and current stress.

6. CONCLUSIONS

In this paper, a novel concept of transformer based energy recovery sustain driver for plasma display panel has been proposed. The proposed topology looks promising as it has lower current stress, better controllability of the resonant inductor and high frequency operation capability.

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