새로운 고효율 플라즈마 디스플레이 패널 분할 서스테인 구동 드라이버

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A new high efficiency splitted sustaining driver for plasma display panel (PDP)

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ABSTRACT

A new High Efficiency splitted sustaining driver for Plasma Display Panel (PDP) is proposed. The proposed circuit is suitable for the large screen PDP. The features of the proposed circuit are zero voltage switching (ZVS) of all main power switches, the reduction of reaction power loss for energy recovering, the stable light emission and simple structure.

1.Introduction

In general, flat panel displays (FPD) are expected to be suitable for a high definition (HD) television. Among them, plasma display panel (PDP) is the most compatible for a large screen HD TV over 50-inch. A PDP market share has increased to the extent that 8~9 million set will be sold in 2006. Demand for the PDP will increase in the future. The PDP is operated with three steps of reset, addressing and sustaining. Most electrical power is consumedin sustaining period because a gray scale, brightness, is made by the number of sustaining pulse [1]. Since the PDP is regarded as a capacitive load (Cp), the EMI noise and considerable energy loss of 2CpVs2 for each cycle must be minimized and the reactive power loss must be reduced by an energy recovery circuit (ERC) [2]. However, as a screen size of the PDP becomes large, there is more gas discharge current and panel capacitance becomes larger. It means increase of power consumption and reactive power loss. To make up for these problems, a new sustaining driver is proposed in this letter. The proposed sustaining driver is operated with divided panel and there are two energy recovery circuits such as a charging energy recovery circuit (CERC) and a discharging energy recovery circuit (DERC) as shown in Fig. 1 (a). As gas discharge current is a half of that in a conventional driver [2], the power consumption can be reduced and stable operation is confirmed in the proposed driver. Also, all power switches in H-bridge can achieve the ZVS with two ERCs. Moreover, the reactive power loss is diminished and light is emitted stably because the proposed circuit has different transition time related to gas discharge with simple structure of the ERC. Since a falling time of the sustaining pulse is not related to gas discharge, the DERC can obtain lower conduction loss in the studied circuit. As a result, the suggested circuit has high efficiency, low EMI noise and good performance.

2. Proposed sustaining driver

Fig. 1 shows the circuit diagram and operational waveforms of the proposed sustaining driver. Since the panel is divided, the two H-bridge is used. As shown in Fig. 1, the CERC is used to make the panel voltage VS or -VS in Y-board and the DERC is used to do the panel voltage 0V in X-board. With two different ERC, the all power switches in H-bridge can be archived the ZVS and the reactive power loss is reduced because the rising time and falling time of sustaining pulse can be obtained differently. The operational principle of the proposed circuit can be explained as follows. It assumed that the voltages of the C1 and C2 are VS/2 and the panel voltages, vcp1 and vcp2, are VS at mode 0.

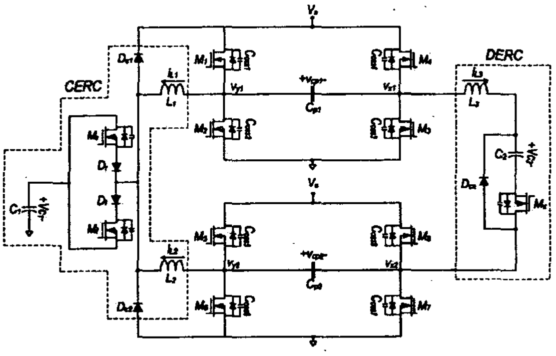
Mode 1 (t0~t1): The mode 1 is begun when MXis turned on and M3 is turned off. With series resonance of panel capacitor Cp1 and inductor L3, the panel voltage of Cp1 becomes 0V at t1. However, the panel voltage of Cp2is sustained in VS.

Mode 2 (t1~t2): When M4 is turned on in condition of ZVS and M7 is turned off, the mode 2 is begun. Because the MX is still turned on, the panel voltage of Cp2 becomes 0V with series resonance of panel capacitor Cp2 and inductor L3. The panel voltage of Cp1 is maintained in 0V.

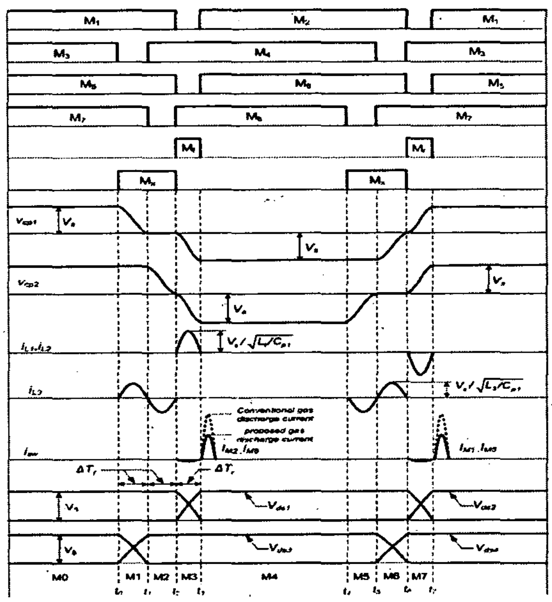
Mode 3 (t2~t3): When M8is turned on in condition of ZVS, Mf is turned on and Mx is turned off, the mode 3 is begun. The panel voltage of Cp2 and Cp1 is increased in -VS with series resonance of Cp1, Cp2, L1 and L2, simultaneously.

Mode 4 (t3~t4): When M2 and M6 are turned on in condition of ZVS and Mf is turned off, mode 4 is begun.

Because the panel voltage of Cp2 and Cpl is fully charged in - VS equally, the gas discharging can be made in two part of PDP. The panel voltage is sustained in - VS after gas discharging.



(a)



(b)

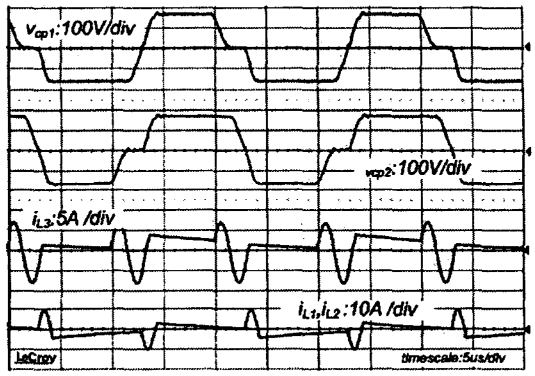
Fig. 1 Proposed new sustaining driver
(a) Circuit diagram (b) Operational waveform

Remained operation is symmetric of the prior mode 1~ mode 4. In Fig.1 (a), diodes Dcl, Dc2, Dcx are used to clamp the drain-source voltage of ERC switches with VS/2 like conventional driver [2]. As explained above, because the gas discharging current is half of that of the conventional sustaining driver, the conduction loss in H-bridge can be reduced. In addition, all main power switches in H-bridge can achieve the ZVS. Moreover, the reactive power loss can be reduced by designing the different transition time without gas discharging problem.

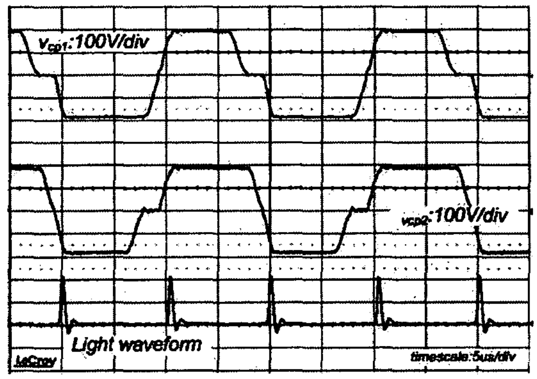
3. Design consideration

To reduce the reactive power loss and to archive the good gas discharging uniformity, the inductance of L1, L2 and L3 is designed by the rising and falling time of the sustaining pulse. To obtain desired the rising time ΔT_r (t2~t3) and the falling time ΔT_f (t0~t1= t1~t2), the inductors are selected as follows at Coss1~Coss8=Coss:

$$L_1=L_2=\frac{1}{C_{p1}+2C_{oss}}\left(\frac{\Delta T_r}{\pi}\right)^2,\quad L_3=\frac{1}{C_{p1}+2C_{oss}}\left(\frac{\Delta T_f}{\pi}\right)^2 \qquad (1)$$



(a)



(b)

Fig. 2 Experimental waveform
(a) Key experimental waveform
(b) Panel voltage and light waveform

4. Experimental results

A prototype of a new sustaining driver is operated at 50kHz with 170V~190V sustaining voltage in 42-inch PDP (about panel capacitor Cpl, Cp2: $40nF$) with following components; H-bridge switch M1~M8: IXYS63N25, Mr, Mf, Mx: IXYS63N25, Dr, Df, Dcl, Dc12 , Dcx : 30CPF06 ,ERC capacitor, Cl and C2 : $2.2\mu F$, inductor L1 and L2 for rising : $1.3\mu H$, inductor L3 for falling : $2.9\mu H$, rising time of sustaining pulse ΔT_r: $1\mu s$ and falling time of sustaining pulse ΔT_f:$1.5\mu s$. Fig. 2 shows experimental results. As shown in Fig. 2 (a), the key experimental waveforms are accord with the theoretical key waveforms. The remained inductor current is neededto charge or discharge parasitic capacitor of diodes and switches. Fig. 2 (b) shows light waveform and panel voltage. When the panel voltages are

190V or - 190V, the light is emitted.

Fig. 3 shows the comparison of power consumption with the conventional driver. The proposed circuit has higher efficiency than that of conventional circuit. The experimental results are to certify the operation and characteristics of the proposed sustaining.

driver.

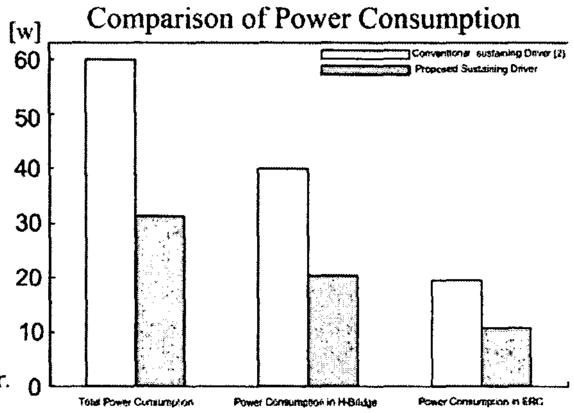


Fig. 3 Comparison of power consumption

5. Conclusion

The new high efficiency sustaining driver for large screen PDP is proposed. The proposed circuit is operated with dividing the panel, so, the conduction loss in H-bridge is reduced. In addition, all power switches in H-bridge can archive the ZVS with the CERC and DERC. Furthermore, the reactive power loss is minimized due to design the rising and falling time of sustaining pulse without affecting gas discharging uniformity. Therefore, the new proposed sustaining driver is expected to be suitable for the large screen high definition (HD) PDP.

Reference

[1] Sobel, A.: 'Plasma Display', IEEE Trans. Plasma Sci, 1991, (6), pp. 1032-1047.

[2] Webber, L.F. and Wood, M.B.: 'Energy recovery sustain circuit for the AC plasma display', S.I.D., 1987, pp 92-95.