전압 스트레스 저감 기법을 적용한 AC-PDP를 위한 단일 유지 구동 회로

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# Single Sustaining Driver for AC-PDP employing Voltage Stress Reduction Technique

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Abstract

Conventional sustaining driver (SD) of plasma display panel (PDP) employing auxiliary circuits on both side of a H-bridge inverter increases volume of PDP with cost. To solve this problem, a new single sustaining driver (SSD), which utilize only one side of auxiliary circuit is proposed. Moreover, using the voltage stress reduction technique (VSRT), the proposed SSD effectively reduces switch voltage stress with a simple structure.

I. Introduction

The PDP, which features a large screen size, wide viewing angle, thinness and high contrast, is very promising for the flat digital display of next generation. The operation of PDP is divided into three periods of setup, addressing and sustaining[1]. Since the panel of PDP features pure capacitive load (Cp) characteristics, excessive surge displacement currents are generated in the sustaining period, resulting in EMI noise and considerable energy loss. To solve this problem, a prior SD has been proposed, which utilize a half resonance between Cp and an external inductor to fully charge and discharge Cp without energy loss[2]. Although this SD shows a good performance, auxiliary circuits employed on both sides of a H-bridge inverter increase volume of PDP with cost. Therefore, a single sustain driver (SSD) concept, which utilize only one side of a prior SD, was suggested to make SD optimize[3]. Fig. 1 shows the circuit diagram and driving waveforms of conventional SSD (Y and X presents the each side voltage of panel). For the stable driving of PDP, VS (gas discharge sustaining voltage) and -VS should be impressed on the panel. In the case of SSD, since it features a half-bridge inverter, main switches suffer from twice a voltage stress (=2VS) compared with that of conventional SD. Therefore, although the conventional SSD can simplify the structure of SD, its twice rated switches results in high cost, high conduction loss and severe heating in return. To solve these problems, a new SSD employing
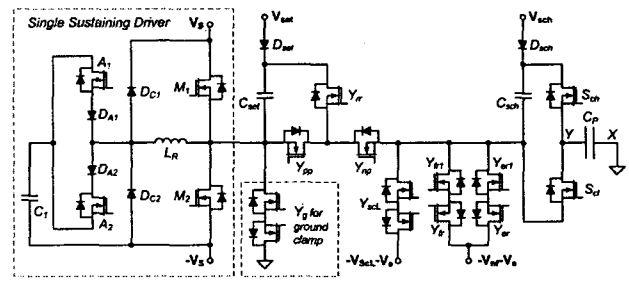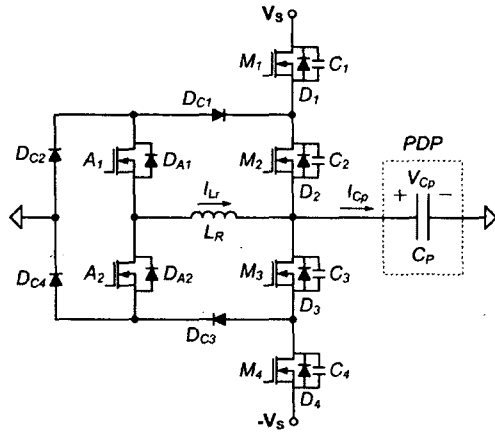

(a) total circuit diagram
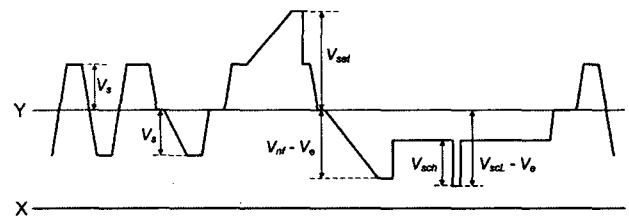
(b) total driving waveform

Fig. 1 Conventional single sustaining dirver

VSRT is proposed in this paper, which effectively reduces switch voltage stress by half in a simple manner. Moreover, additional bidirectional switch Yg of conventional SSD to maintain the panel voltage at ground is not needed in the proposed SSD, since its structure potentially offers a solution to achieve this operation without an auxiliary circuitry.

II. Proposed SSD

Fig. 3 shows the circuit diagram and key waveforms of proposed SSD. The based circuit of proposed SSD is a multi-level half-bridge inverter that consists of 4 main switches, M1, M2, M3 and M4. A bidirectional switch for an energy recovery action consists of A1, A2, DC2 and DC4. DC1, DC2, DC3 and DC4 act for clamp diodes to limit voltage stress of outer main switches M1 and M4. The main concept of VSRT is ensuring all switch voltages of a multi-level half-bridge inverter at VS by simply adjusting the gate signals with clamp diodes. That is, inner switches (M2, M3) are turned off lagging

(a) circuit diagram
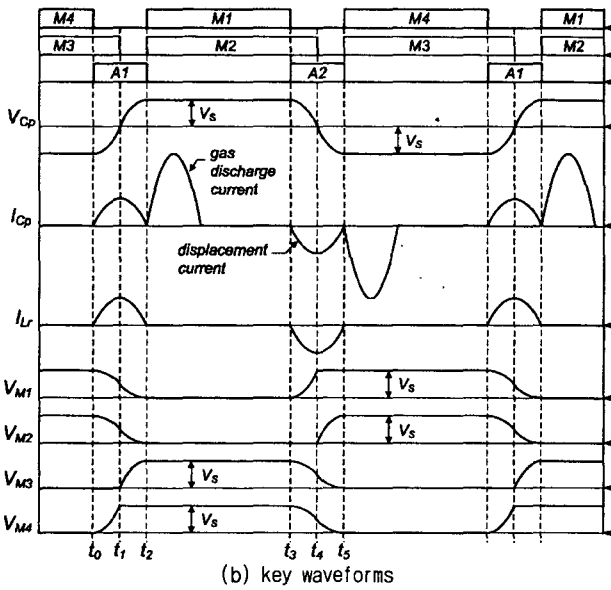
(b) key waveforms

Fig. 2 Proposed SSD employing VSRT

to the outer switches (M1, M4) to charge outer switches first in transitions. Therefore, outer switches are clamped to VS by clamp diodes and then inner switches reach VS. By this method, both inner and outer switches effectively ensure voltage stresses at VS, and those of other auxiliary devices are also ensured at VS. Moreover, it shows an additional advantage that VCp can be maintained at the ground through the inner switches and clamp diodes without any additional circuit.

The operation of one switching cycle is subdivided into six modes as shown in Fig. 2(b) and mode diagrams are presented in Fig. 3. Since the operational principle of two half cycles are symmetric, only the first cycle is explained. Before t0, M3 and M4 are conducting and VCp maintains -VS.

Mode 1 (t0 ~ t1): When M4is turned off and A1 is turned on at t0, mode 1 begins. As can be seen in Fig. 3(a), since there forms a current path through DC2 and A1, the resonance between Cp and LR is occurred. Since
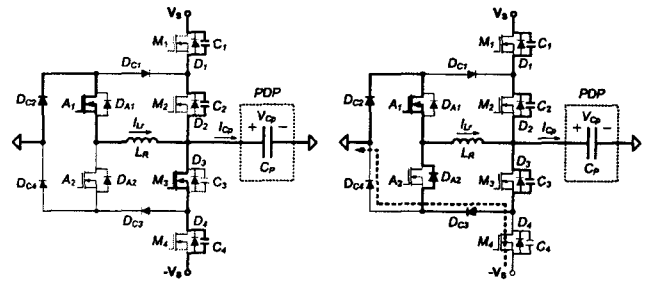
(a) Mode 1 (t0 ~ t1)   (b) Mode 2 (t1 ~ t2)
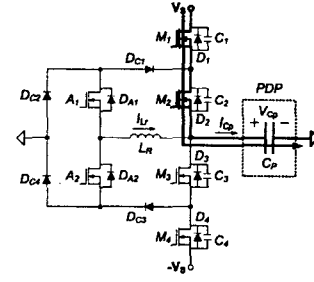
(c) Mode 3 (t2 ~ t3)

Fig. 3 Mode diagrams of proposed SSD

M3 still conducts, only C4 is charged accordingly with the increase of VCp, and C1 and C2 are discharged.

Mode 2 (t1 ~ t2): After a quarter resonant cycle, M3 is turned off and mode 2 begins at t1. As shown in Fig. 3(b), VM4 is clamped to VS by clamp diodes DC3 and DC4 (dot line represents clamp path). Cp is continuously resonated with LR through DC2 and A1. Since VM4 is clamped to VS, only C3 is charged with the increase of VCp, and C1 and C2 are discharged.

Mode 3 (t2 ~ t3): After a quarter resonant cycle, VM3 and VCp reach VS at t2 and mode 3 begins. Since VM1 and VM2 reach 0V, M1 and M2can be turned on with zero-voltage-switching (ZVS). As shown in Fig 3(c), during this mode, the gas discharge current to emit visible light is supplied to the panel through M1 and M2.

The gas discharge of PDP is very sensitive to the transition time dT, and it affects panel brightness and discharge stability. dT is defined as the time during which VCp is changed between VS and -VS. If dT is equal to a half cycle of the resonance between Cp and LR, the value of LR for dT can be expressed as $LR = (dT/\pi)2/Cp$

III. Experimental results

The prototype of proposed SSD has been built for a one sixth of 42inch PDP (Cp=10nF) with following specifications: VS=200V, switching frequency = 50kHz, LR = 10uH, M1-M4 and A1-A2 = 2SK2995, DC1-DC4 = STTH2003 and dT = 1usec. Although, the device count of proposed SSD is larger than that of conventional one, cost and conduction loss can be reduced with half rating

switches. Fig. 4 shows the key experimental waveforms of proposed SSD, which illustrates that the energy of CP is recovered and the voltage stresses of all switches are well maintained at VS. Fig. 5 presents the detailed waveforms of switch voltage during each transition, which is agreed well with the theoretical operation.
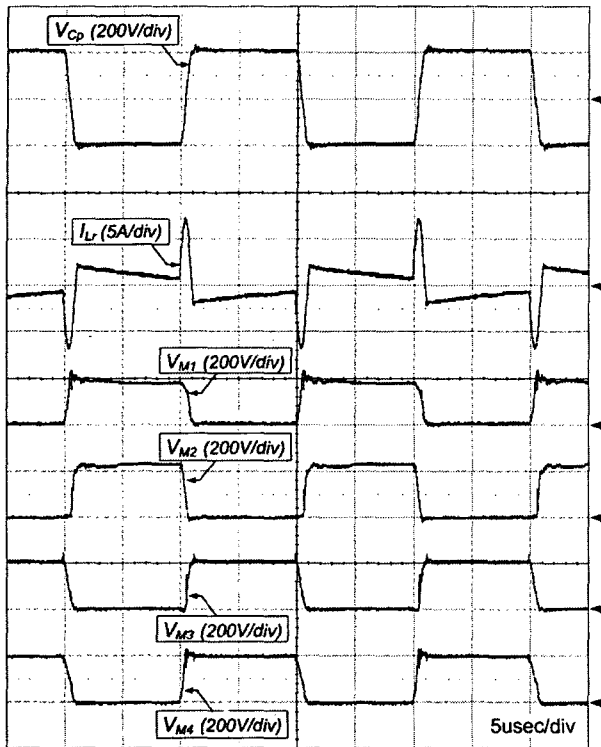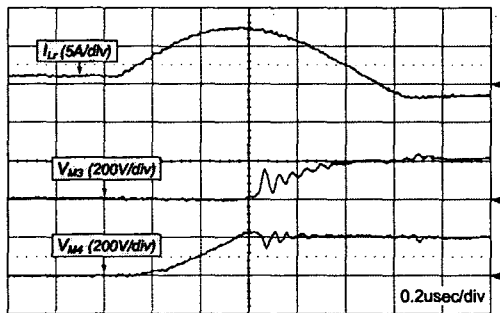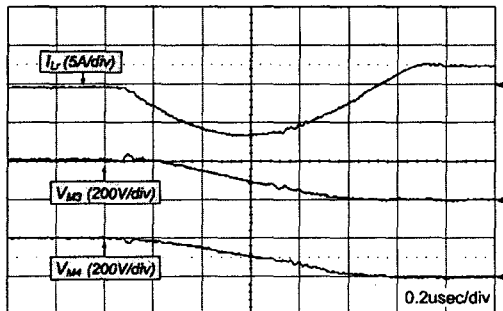

Fig. 4 Key experimental waveforms

(a) rising waveform of VM3 and VM4

(b) falling waveform of VM3 and VM4

Fig. 5 Voltage waveforms of switches during transitions

IV. Conclusion

A new SSD employing VSRT, which effectively reduces switch voltage stress in a simple manner, is proposed. Adjusting the gate timing of switches with clamp diodes, switch voltage stress is effectively ensured at VS, which may lead to reduced cost, conduction loss and heating. Moreover, it offers a solution to maintain panel voltage at ground without an additional circuitry and ZVS of main switches is well achieved. Therefore, the proposed SSD employing VSRT features low cost, high performance and simple structure.

References

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