New Multi-Output LLC Resonant Converter for High Efficiency and Low Cost PDP Power Module

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ABSTRACT

A new multi-output LLC resonant converter is proposed for high efficiency and low cost plasma display panel (PDP) power module. In the proposed converter, zero-voltage (ZV) turn-on of the primary MOSFETs and zero-voltage (ZC) turn-on and turn-off of the secondary diodes are guaranteed in the overall input voltage and output load ranges. In addition, the primary MOSFETs and the secondary diodes have the low voltage stresses clamped to input and the output voltages, respectively. Therefore, the proposed converter shows the high efficiency due to the minimized switching and conduction losses. Moreover, by employing the transformer with multiple secondary windings, the proposed converter can have multiple outputs, which show the great cross-regulation characteristics. Therefore, the proposed converter is suitable for high efficiency and low cost PDP power module.

I. INTRODUCTION

PDPs show many desired features as a display device, such as large screen size, wide view angle, fast response, high contrast, thinness, and long life time. Moreover, recently, the power consumption is greatly decreased through the auto power control (APC) technique, and the cost per inch is also reduced by the application-specific integrated circuit (ASIC) technology and the improvement of the panel fabrication process. Therefore, PDPs show the brightest prospect as a flat display panel.

PDPs are operated in three periods of resetting, addressing, and sustaining within a sub-field, in order to display the desired images. In resetting period, the wall charges of the overall PDP cells are removed by applying the resetting ramps to the scanning and sustaining electrodes. And then, to create the wall charges at the required PDP cells, the data and scanning pulses are applied to the addressing and scanning electrodes, respectively. If the continuous sustaining pulses are applied between the scanning and sustaining electrodes during the sustaining period, the selected PDP cells emit the intense light and the desired image can be displayed.

Therefore, to drive PDPs optimally, the various power supplies are required, such as the sustaining, addressing, scanning, and resetting power supplies. PDP power module includes not only these power supplies but also the logic circuit power supply, as shown in Fig. 1. In addition, the boost pre-regulator for power factor correction (PFC) is implemented at input stage. Thus, PDP power module has the complicated structure and the high power rating, especially, the sustaining and addressing power supplies have the highest power rating. However, as described above, the sustaining and addressing power supplies do not operate at the same time. Therefore, the sustaining and addressing power supplies can be implemented as a single power stage with dual outputs, and then the high power density and the low cost of PDP power module can be obtained.

In this paper, a new LLC resonant converter suitable for multiple output applications is proposed. The operational principles of the proposed converter are analyzed and the cross-regulation characteristics for dual outputs are investigated. Moreover, the 440W prototypes of the proposed converter are implemented for the sustaining and addressing power supplies and their operations and performances are investigated.

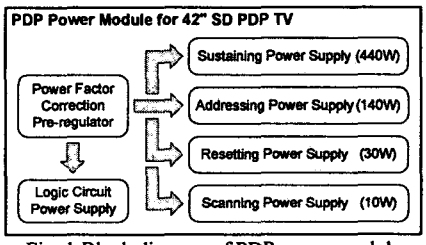


Fig. 1 Block diagram of PDP power module

II. PRINCIPLES OF OPERATION

As shown in Fig. 2, the proposed converter consists of two half-bridge cells as the input and output stages, symmetrically. The input and output stages are connected by the resonant cell, which is composed of the series resonant inductor L_R, the series resonant capacitor C_R, and the transformer T_1. Moreover, the transformer includes the magnetizing inductor L_M, and it works as the parallel resonant inductor.

A. Mode analysis

The proposed converter operates in six modes according to the switching states of the primary MOSFETs and the secondary diodes, and the key waveforms are presented in Fig. 3. Before t_0, since D_{SA} and D_{SB} are turned-off, the transformer secondary current i_{SEC} is zero. The transformer primary current i_{PRI} flows reversely through Q_A and it equals the transformer magnetizing current i_{LM}.

Mode 1 (M_1, t_0~t_1): When Q_A is turned-off at t_0, mode 1 begins. Since i_{PRI} has the negative initial current, it discharges the parasitic output capacitor of Q_M and charges that of Q_A. When $v_{DS}(Q_M)$ is decreased to $(1/2)[V_S-(N_P/N_S)V_O-2v_R]$, D_{SA} is turned-on and i_{LM} is linearly increased by the applied voltage of $(1/2)(N_P/N_S)V_O$. At the same time, L_R and C_R resonate with the applied voltage of $(1/2)[V_S-(N_P/N_S)V_O-v_{DS}(Q_M)]$. Provided that the gate signal is applied to Q_M after the parasitic output capacitor of Q_M is fully discharged, ZVS turn-on of Q_M can be obtained.

Mode 2 (M_2, t_1~t_2): When ZVS operation of Q_M is finished and i_{PRI} is increased to zero, mode 2 begins at t_1. In mode 2, D_{SA} maintains turn-on state and i_{LM} is linearly increased by the applied voltage of $(1/2)(N_P/N_S)V_O$, as same as mode 1. Since $v_{DS}(Q_M)$ is zero, L_R and C_R resonate with the applied voltage of $(1/2)[V_S-(N_P/N_S)V_O]$.

Mode 3 (M_3, t_2~t_3): When i_{PRI} becomes equal to i_{LM} and then i_{SEC} is zero, D_{SA} is turned-off and mode 3 begins at t_2. L_M, L_R, and C_R resonate with the applied voltage of $(1/2)V_S$, and i_{PRI} maintains equal to i_{LM} in mode 3. When Q_M is turned-off at t_3, mode 4 begins. The operations of mode 4, 5, and 6 are symmetrically same as those of mode 1, 2, and 3, respectively.

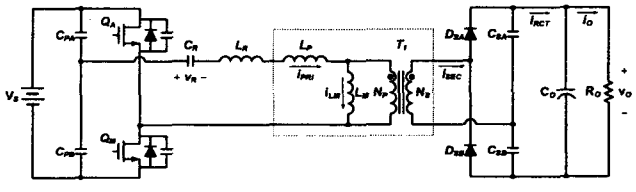


Fig. 2 Circuit diagram of the proposed converter

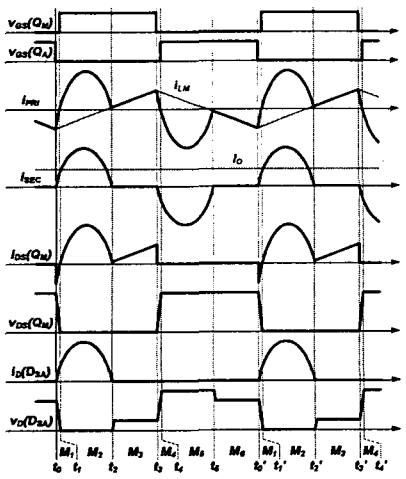


Fig. 3 Key waveforms of the proposed converter

B. Input-output voltage gain ratio

Using the fundamental component simplification (FCS) method, we can derive the input-output voltage gain of the proposed converter given by

$$G_{DC}=\frac{V_O}{V_S}=\frac{\frac{N_S}{N_P}}{\sqrt{\left\{1+k\left[1-\left(\frac{F_R}{F_S}\right)^2\right]\right\}^2+\left[\left(\frac{F_S}{F_R}-\frac{F_R}{F_S}\right)Q\right]^2}}, \quad (1)$$

where $k=L_R/L_M$, $F_R=1/\left(2\pi\sqrt{L_RC_R}\right)$, $Q=\sqrt{(L_R/C_R)}/R_{ac}$, $R_{ac}=2R_O\left(N_P/N_S\right)^2/\pi^2$, and F_S is the switching frequency. In Fig. 4, the input-output voltage gain is plotted as a function of the ratio F_S to F_R, with the circuit parameters of L_R=12μH, L_M=200μH, C_R=100nF, and N_P:N_S=1:1.

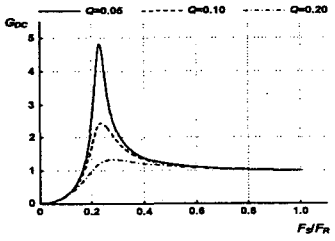


Fig. 4 Input-output voltage gain of the proposed converter

C. Advantages of proposed converter

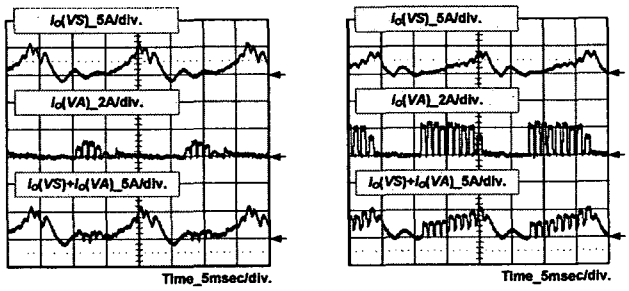
The proposed converter has many advantages and they are described as follows: i) Two half switching cycles are well balanced each other due to the half-bridge capacitors in the input and output stages. Thus, the resonant currents of the primary and secondary sides have low peak values. Moreover, No magnetizing current offset exists in the transformer. ii) The primary MOSFETs are turned-on under ZV condition, and the secondary diodes are turned-on and turned-off under ZC condition. iii) The primary MOSFETs and the secondary diodes have the low voltage stresses clamped to the input and output voltages, respectively. Therefore, thank to the minimized conduction and switching losses, the proposed converter can achieve high efficiency and high power density.

III. Cross-Regulation Characteristics

To apply the proposed converter to the sustaining power supply VS and the addressing power supply VA of PDP power module, the load characteristics of these power supplies are investigated and the cross-regulation characteristics of the proposed converter are analyzed.

A. Load characteristics of the sustaining and addressing outputs

The load currents and resistances of the sustaining and addressing power supplies are changed variously according to the displayed images of PDP. Fig. 5 shows the load currents of these power supplies at those images of PDP. The sustaining power supply has the heaviest load condition at full white image and the addressing power supply does at dot on/off image [1,2]. However, at these images, both the sustaining and the addressing power supplies do not have the heaviest load condition, simultaneously. That is, the addressing power supply has the light load condition at full white image and the sustaining power supply does at dot on/off image. At other images, both the sustaining and addressing power supplies have the moderate load condition. Furthermore, the sustaining and addressing power supplies do not operate at the same time. In other words, at a given image, the load currents of these power supplies are distributed periodically and alternatively. Therefore, the sustaining and addressing power supplies can be implemented as a single power stage with dual outputs.



(a) Full white image (b) Dot on/off image

Fig. 5 Load current waveforms of PDP power module

B. Scheme 1: independent outputs

For dual outputs, the circuit diagram of the scheme 1 is shown in Fig. 6. The transformer T_1 consists of one primary winding and two secondary windings. In addition, the secondary windings have the respective leakage inductances.

Therefore, using the FCS method with the secondary leakage inductors L_{S1} and L_{S2}, we can derive the input-output voltage gains as follows:

$$G_{DC1}=\frac{V_{O1}}{V_S}=\frac{N_{S1}}{N_P}\frac{R_{O1}/\pi^2}{\sqrt{\left(R_{O1}/\pi^2\right)^2+\left(\pi L_{S1}F_S\right)^2}}G_{COM}, \quad (2)$$

$$G_{DC2}=\frac{V_{O2}}{V_S}=\frac{N_{S2}}{N_P}\frac{R_{O2}/\pi^2}{\sqrt{\left(R_{O2}/\pi^2\right)^2+\left(\pi L_{S2}F_S\right)^2}}G_{COM}, \quad (3)$$

where G_{COM} is given by the equation (4),

$R_{ac}=R_{O1,ac}//R_{O2,ac}$, $R_{O1,ac}=2R_{O1}\left(N_P/N_{S1}\right)^2/\pi^2$,

$R_{O2,ac}=2R_{O2}\left(N_P/N_{S2}\right)^2/\pi^2$, $\alpha=\left(\pi^4L_{S1}L_{S2}\right)/\left(4R_{O1}R_{O2}\right)$,

$\beta=\pi^2\left(L_{S1}/R_{O1}+L_{S2}/R_{O2}\right)/2$, and

$\gamma=\pi^4\left(L_{S1}/N_{S1}+L_{S2}/N_{S2}\right)\left(N_{S1}N_{S2}/N_P\right)^2/\left(4R_{O1}R_{O2}\right)$.

$$G_{COM}=\frac{\left(1-4\pi^2\alpha F_S^2\right)^2+4\pi^2\beta^2F_S^2}{\sqrt{\left[1+k\left(1-\frac{F_R^2}{F_S^2}\right)+4\pi^2k\alpha\left(F_R^2-F_S^2\right)+\frac{\alpha}{C_R}-4\pi^2L_P\gamma F_S^2\right]^2+\left[\left(\frac{F_S}{F_R}-\frac{F_R}{F_S}\right)Q+\left(k\frac{F_S}{F_R}-\frac{F_R}{F_S}\right)2\pi\beta F_R\right]^2}} \quad (4)$$

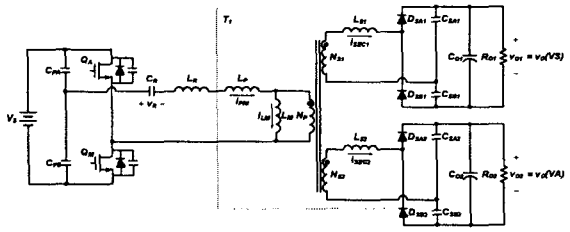


Fig. 6 Circuit diagram of scheme 1 for dual outputs

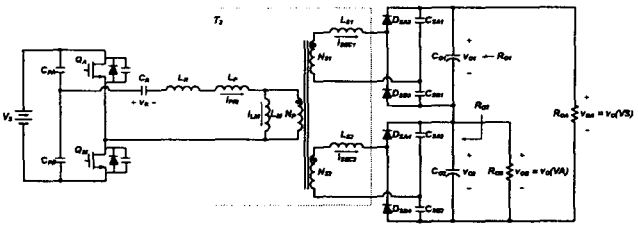


Fig. 7 Circuit diagram of scheme 2 for dual outputs

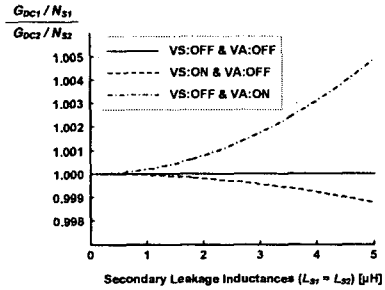


Fig. 8 Voltage gain ratio of scheme 1 according to load condition

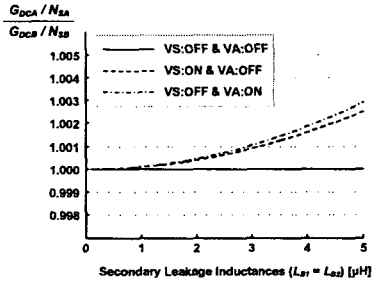


Fig. 9 Voltage gain ratio of scheme 2 according to load condition

In the ideal case that the leakage inductances of the transformer secondary windings are zero, the voltage gain ratio G_{DC1}/G_{DC2} is exactly equal to the turns ratio of the transformer secondary windings N_{S1}/N_{S2}, irrespective of the other conditions, as shown in the equations (2) and (3). Therefore, the cross-regulation of both outputs is guaranteed in the ideal case. On the other hand, the transformer has the leakage inductances in the secondary windings as well as the primary one in the practical case, consequently, the voltage gain ratio is not equal to the turns ratio of the transformer secondary windings, and it depends not only on the turns ratio but on the secondary leakage inductances and the load resistances. The voltage gain ratio normalized by turns ratio is plotted in Fig. 7 as functions of the secondary leakage inductances with the circuit parameters of L_R = 12μH, L_M = 200μH, C_R = 100nF, F_S = 100kHz, and N_P: N_{S1}:N_{S2} = 25:10:4.

C. Scheme 2: series-connected outputs

Like scheme 1, the circuit diagram of the scheme 2 for dual outputs is shown in Fig. 5. The transformer T_1 consists of one primary winding and two secondary windings, which have the respective leakage inductances. Moreover, two outputs v_{O1} and v_{O2} are series-connected, and new outputs v_{OA} and v_{OB} are formed, as shown in Fig. 8. Therefore, the following equations can be defined.

$$v_{OA} = v_{O1} + v_{O2}, \quad v_{OB} = v_{O2}, \quad N_{SA} = N_{S1} + N_{S2}, \quad N_{SB} = N_{S2},$$

$$R_{O1} = \frac{V_{O1}}{V_{OA}} R_{OA} \cong \frac{N_{S1}}{N_{SA}} R_{OA}, \text{ and } R_{O2} = R_{OB} // \left(\frac{V_{O2}}{V_{OA}} R_{OA} \right) \cong R_{OB} // \left(\frac{N_{S2}}{N_{SA}} R_{OA} \right).$$

Using the FCS method with the above-defined parameters and the secondary leakage inductors, the input-output voltage gain equations can be obtained as the following equations (5) and (6).

$$G_{DCA} = \frac{V_{OA}}{V_S} = G_{DC1} + G_{DC2}, \tag{5}$$

$$G_{DCB} = \frac{V_{OB}}{V_S} = G_{DC2}, \tag{6}$$

where G_{DC1} and G_{DC2} are defined in the equations (2) and (3). Similar to scheme 1, the cross-regulation of both outputs is guaranteed in the ideal case. Moreover, the voltage gain ratio G_{DCA}/G_{DCB} is also affected not only by the turns ratio N_{SA}/N_{SB} but by the leakage inductances and the load resistances in the practical case. Therefore, to obtain the excellent cross-regulation characteristics, the secondary leakage inductances must be minimized. The voltage gain ratio normalized by turns ratio are plotted in Fig. 9 as functions of the secondary leakage inductances with the circuit parameters of L_R = 12μH, L_M = 200μH, C_R = 100nF, F_S = 100kHz, and N_P: N_{S1}:N_{S2} = 25:6:4. As shown in Fig. 7 and Fig. 9, scheme 2 has the better cross-regulation characteristics, compared with scheme 1. Furthermore, scheme 2 can improve the transformer utilization efficiency and requires the lower voltage rating of the secondary diodes than scheme 1. As a result, scheme 2 of the proposed converter shows higher efficiency and lower cost as well as better cross-regulation characteristics.

IV. Experimental Results

To verify the operational principles and the cross-regulation characteristics of the proposed converter, two 440W prototypes of scheme 1 and 2 are implemented for the sustaining and addressing power supplies of PDP power module and only the sustaining output is controlled by feedback loop. Their design specifications are presented in TABLE I. In addition, TABLE II shows the key circuit parameters for scheme 1 and 2. The respective transformers T_1 and T_2 have the different turns ratio and secondary leakage inductances. Moreover, scheme 2 employs the lower voltage rating secondary diodes.

TABLE I
Design Specifications for PDP Power Module

Input Voltage, V_S		385VDC
Sustaining Power Supply	Regulated Output Voltage, V_O(VS)	175V
	Maximum Load Current, $I_{O,max}$(VS)	2.5A
	Maximum Output Power, $P_{O,max}$(VS)	440W
Addressing Power Supply	Nominal Output Voltage, V_O(VA)	70V
	Maximum Load Current, $I_{O,max}$(VA)	2.0A
	Maximum Output Power, $P_{O,max}$(VA)	140W

TABLE II
Key Circuit Parameters for Scheme 1 and Scheme 2

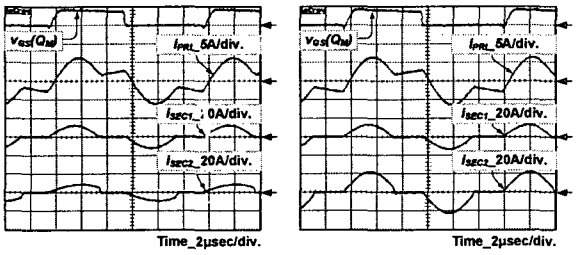
Primary MOSFETs, Q_M and Q_A		FQA24N60 (600V, 24A)
Resonant Inductor, L_R		12μH
Resonant Capacitor, C_R		47μF, 630V, 2EA
T_1	Turns Ratio, N_P : N_{S1} : N_{S2}	25 : 10 : 4
	Primary Magnetizing Inductor, L_M	200μH
	Primary Leakage Inductor, L_P	4.64μH
	Secondary Leakage Inductor 1, L_{S1}	0.34μH
	Secondary Leakage Inductor 2, L_{S2}	0.09μH
Secondary Diodes, D_{SA1} and D_{SB1}		STTH2003(300V, 20A)
Secondary Diodes, D_{SA2} and D_{SB2}		STPS20100(100V, 20A)
T_2	Turns Ratio, N_P : N_{S1} : N_{S2}	25 : 6 : 4
	Primary Magnetizing Inductor, L_M	198μH
	Primary Leakage Inductor, L_P	4.33μH
	Secondary Leakage Inductor 1, L_{S1}	0.07μH
	Secondary Leakage Inductor 2, L_{S2}	0.06μH
Secondary Diodes, D_{SA3} and D_{SB3}		STPS20150(150V, 20A)
Secondary Diodes, D_{SA4} and D_{SB4}		STPS20100(100V, 20A)

A. Experiment of the proposed converter

The key current waveforms of scheme 1 and 2 are shown in Fig. 10 at full load condition (580W), and they are well-agreed to the theoretical waveforms of Fig. 3 and well-balanced around zero. In addition, scheme 1 and 2 show the same primary current waveforms, but the different secondary current waveforms according to the output connections. Fig. 11 shows the key switching waveforms of scheme 1 and 2. In both schemes, the primary MOSFETs are turned-on under ZV condition, and the secondary diodes are turned-on and turned-off under ZC condition. Moreover, the voltage stresses of the secondary diodes are clamped to V_{O1} and V_{O2}, and D_{SA3} and D_{SB3} of scheme 2 has much lower voltage stress than D_{SA1} and D_{SB1} of scheme 1, as shown in Fig. 11. Finally, the measured efficiencies of scheme 1 and 2 are 96.21% and 96.69%, respectively, at full load condition.

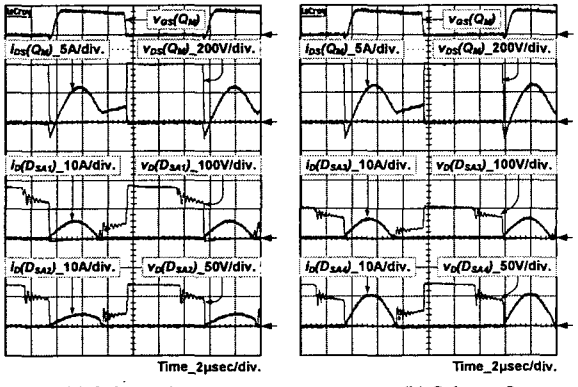
B. Experiment for the cross-regulation characteristics

Above all, the cross-regulation characteristics of the proposed converter are investigated at the static (DC) load condition. Fig. 12(a) shows the variation of the addressing output voltage as a function of the sustaining output current under the zero addressing output current condition. On the contrary, the variation of the addressing output voltage is plotted in Fig. 12(b) as a function of the addressing output current under the zero sustaining output current condition. The maximum variation of the addressing output voltage is measured to 5.42V (7.93%) of scheme 1 and 1.97V (2.88%) of scheme 2. As investigated, scheme 2 shows the better cross-regulation characteristics than scheme 1 at the static (DC) load condition.



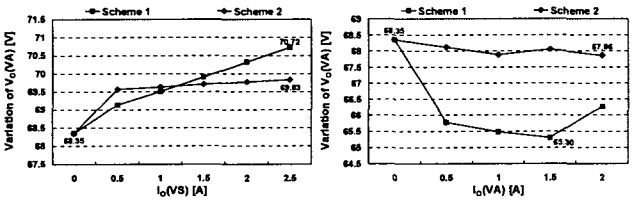
(a) Scheme 1 (b) Scheme 2

Fig. 10 Key experimental current waveforms



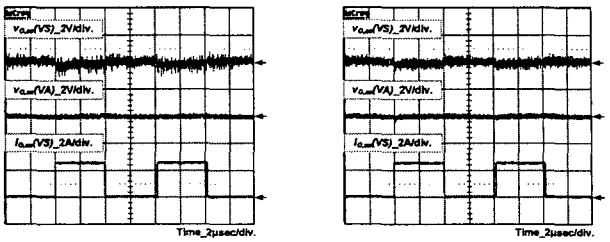
(a) Scheme 1 (b) Scheme 2

Fig. 11 Key experimental switching waveforms



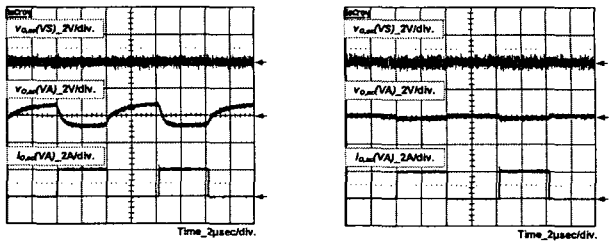
(a) Varying $I_O(VS)$ (b) Varying $I_O(VA)$

Fig. 12 Cross-regulation at the static load condition



(a) Scheme 1 (b) Scheme 2

Fig. 13 Cross-regulation at the dynamic load condition varying $i_O(VS)$



(a) Scheme 1 (b) Scheme 2

Fig. 14 Cross-regulation at the dynamic load condition varying $i_O(VA)$

Furthermore, the cross-regulation characteristics at the dynamic (AC) load condition are examined. First, the pulsating square current from zero to maximum 2.5A is imposed on the sustaining output under the zero addressing output current condition. Fig. 13 shows its resulting waveforms. In both schemes, the sustaining and addressing output voltages are well regulated, because the sustaining output is controlled by feedback loop and the addressing output has no load current. Next, the variation of the addressing output voltage is presented in Fig. 14, imposing the pulsating current from zero to maximum 2.0A on the addressing output under the zero sustaining output current condition. Since the addressing output of scheme 1 is not controlled and has pulsating output current, the addressing output shows the voltage variation of 1.8V (2.74%), as can be seen in Fig. 14(a). On the other hand, the addressing output of scheme 2 has the much smaller voltage variation below 0.5V (0.74%). Therefore, scheme 2 shows the excellent cross-regulation characteristics at the dynamic (AC) load condition, too. Finally, the cross-regulation characteristics of scheme 2 are experimentally verified by applying to 42-inch SD PDP TV at full white image. The measured voltage variations of the sustaining and addressing outputs are 1.76V (1.01%) and 0.73V (1.04%), respectively. This is the reasonable variation enough to guarantee the good operation of PDP TV.

V. CONCLUSIONS

In this paper, a new multi-output LLC resonant converter is proposed for high efficiency and low cost PDP power module. The proposed converter guarantees the soft switching of the primary MOSFETs and the secondary diodes in the overall input voltage and output load ranges. Moreover, the primary MOSFETs and the secondary diodes have low voltage stresses clamped to input and the output voltages, respectively. Therefore, the proposed converter shows the high efficiency about 97% due to the minimized switching and conduction losses. The proposed converter shows the excellent cross-regulation characteristics and these are confirmed experimentally. The proposed converter is expected to be suitable for the high efficiency and low cost PDP power module and other multi-output applications.

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