# PDP을 위한 새로운 저가형 에너지 회수 회로

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# A new low-cost energy-recovery circuit for a plasma display panel

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## ABSTRACT

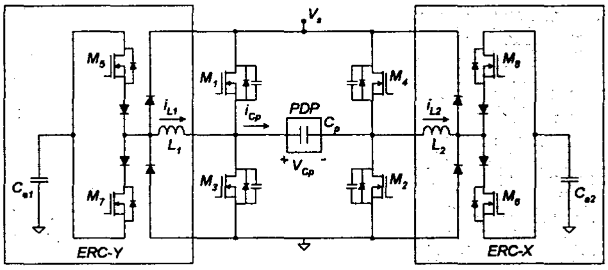
A new low-cost energy-recovery circuit (ERC) for a plasma display panel (PDP) is proposed. It has two auxiliary switches clamped on a half sustain voltage, and inductor currents are built up before the PDP is charged and discharged. Therefore, it features a low cost, fully charged/discharged PDP, zero voltage switching (ZVS), low electromagnetic interference (EMI), low current stress, no severe voltage notch, and high energy-recovery capability.

## 1. Introduction

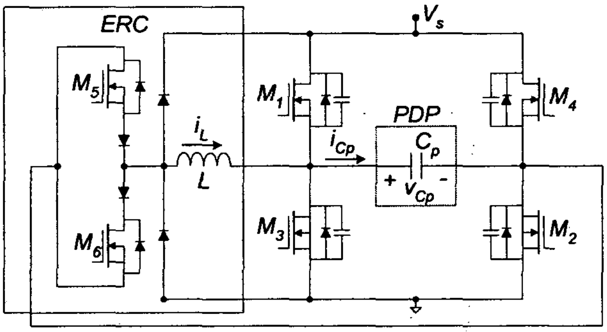
Since the PDP has advantages such as a wide view angle, lightness, thinness, high contrast, and large screen, it is one of the most leading candidates for large screen TVs. Generally, the PDP can be equivalently regarded as a capacitance load $C_p$. Therefore, when a sustain voltage $V_s$ is alternatively applied across the PDP using full bridge inverter, there are the considerable energy loss of $2C_pV_s^2$ per each cycle, excessive surge current, and severe EMI noise.

To solve these problems, several approaches have been proposed. Among them, Weber's circuit shown in Fig. 1(a) features a low conduction loss and high performance [1]. However, it has several disadvantages. There is a severe voltage drop across a parasitic resistance, which results in the serious hard switching, excessive surge current, serious power dissipation, severe EMI noise, and poor energy-recovery capability. Also, a large gas-discharge current causes a serious voltage notch across the PDP. Above all, it uses four auxiliary switches having voltage stress of $V_s/2$, which results in high cost.

Sakai's circuit shown in Fig. 1(b) features a simple structure and good energy-recovery performance [2]. However, it still has disadvantage that voltage drop due to a parasitic resistance causes the serious hard switching, severe voltage notch, excessive surge current, serious power dissipation, severe EMI noise, and poor energy-recovery capability. Moreover, voltage stress of two auxiliary switches in ERC is $V_s$, which results in high cost.



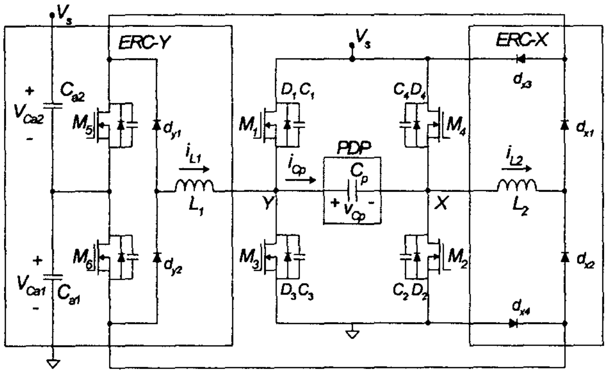
(a) Weber's circuit



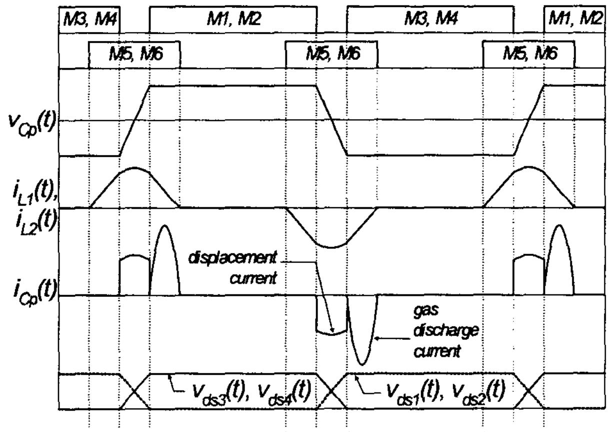
(a) Sakai's circuit

Fig. 1 Prior circuits

To overcome these drawbacks of prior circuits, A new low-cost ERC for the PDP is proposed as shown in Fig. 2(a). Since the proposed circuit has two auxiliary switches clamped on $V_s/2$ instead of four auxiliary switches clamped on $V_s/2$ for Weber's circuit and two auxiliary switches clamped on $V_s$ for Sakai's circuit, it features a lower cost of the production compared with prior circuits. Furthermore, the inductor currents are built up before the PDP is charged and discharged. These built-up inductor currents help to fully charge and discharge the PDP with fast transition time, achieve ZVS of main switches, and reduce the EMI noises. In particular, since these compensate for a large gas-discharge current, there is no severe voltage notch, and the current stress of main switches can be reduced effectively. Therefore, the proposed circuit features the high energy-recovery capability.



(a) Proposed circuit



(b) Key waveforms

Fig. 2 Proposed circuit and its key waveforms

## 2. Operation of the proposed circuit

Fig. 2(b) shows key waveforms of the proposed circuit. One cycle operation is divided into six modes. It is assumed that $C_1$, $C_2$, $C_3$ and $C_4$ are equal to $C_{oss}$, $V_{Ca1}$ and $V_{Ca2}$ are equal to $V_s/2$, and $L_1$ and $L_2$ are equal to L.

***Mode 1($t_0$~$t_1$):*** When $M_5$ and $M_6$ are turned on at $t_0$, mode 1 begins. Since $V_s/2$ is applied across $L_1$ and $L_2$, $i_{L1}$ and $i_{L2}$ increase linearly with slope of $V_s/(2L)$.

***Mode 2($t_1$~$t_2$):*** When $M_3$ and $M_4$ are turned off at $t_1$, mode 2 begins. $L_1$ and $L_2$ begins to charge $C_p$, $C_3$ and $C_4$, and discharge $C_1$ and $C_2$ with initial conditions of $v_{Cp}(t_1)=-V_s$ and $I_{L0}=i_{L1}(t_1)=i_{L2}(t_1)=V_s(t_1-t_0)/(2L)$ as follows:

$$v_{Cp}(t)=-V_s\cos\omega(t-t_1)+I_{L0}\sqrt{\frac{2L}{C_p+C_{oss}}}\sin\omega(t-t_1) \quad (1)$$

where $\omega=[1/\{2L(C_p+C_{oss})\}]^{0.5}$. As shown in equation (1), $v_{Cp}$ increases from $-V_s$ by resonance between 2L and $(C_p+C_{oss})$. And then, when $v_{Cp}$ is clamped on $V_s$, the gas-discharge begins to take place. $i_{L1}$ decreases linearly with slope $-V_s/(2L)$ through $C_{a1}$, $M_6$, $d_{y2}$ and $D_1$. $i_{L2}$ decreases linearly with slope $-V_s/(2L)$ through $D_2$, $d_{x1}$, $M_5$, and $C_{a2}$. Therefore, $M_1$ and $M_2$ can be turned on under ZVS, and $C_p$ is fully charged to $V_s$.

***Mode 3($t_2$~$t_3$):*** When $M_1$ and $M_2$ are turned on at $t_2$, mode 3 begins. $i_{L1}$ fed back to an input voltage source through $C_{a1}$, $M_6$, $d_{y2}$ and $M_1$ compensates for a large part of the gas-discharge current through $M_1$, and $i_{L2}$ fed back to an input voltage source through $M_2$, $d_{x1}$, $M_5$, and $C_{a2}$ compensates for a large part of the gas-discharge current through $M_2$. Therefore, the current stress of $M_1$ and $M_2$ can be considerably reduced as well as the voltage notch across the PDP can be effectively overcome. In this mode, when $i_{L1}$ and $i_{L2}$ decrease to zero, $M_5$ and $M_6$ are turned off. Voltages across $M_5$ and $M_6$ are clamped on $V_s/2$ due to $C_{a1}$ and $C_{a2}$, which results in a low cost.

Therefore, the proposed circuit features the fully charged/discharged PDP, ZVS of main switches, no severe hard switching, less power dissipation, low surge current, and low EMI noise due to built-up inductor currents. Furthermore, it shows the high energy-recovery capability.

The circuit operation of $t_3$~$t_6$ is symmetric to that of $t_0$~$t_3$.

## 3. Design considerations

Since the brightness of a PDP depends on the operation frequency and transition time, the transition time $T_d=t_2-t_1$ $(=t_5-t_4)$ is required to be as fast as possible. The built-up time, $\Delta t_L=t_1-t_0$ $(=t_4-t_3)$, of $L=L_1=L_2$ can be determined from the equation (1) as follows:

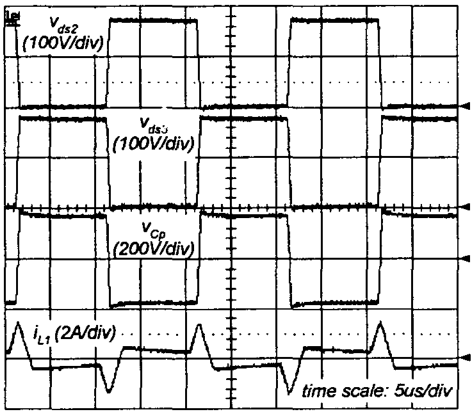
$$\Delta t_L=\frac{\sqrt{2L(C_p+C_{oss})}}{\tan[T_d/(2\sqrt{2L(C_p+C_{oss})})]} \quad (2)$$

## 4. Experimental results

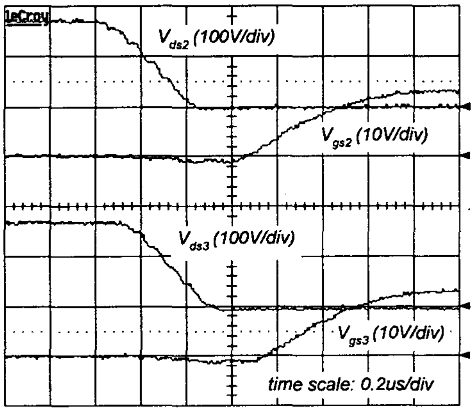
To verify the behavior and analysis of the proposed circuit, the prototype circuit is implemented with specifications of $f_s$=50kHz, $C_p$=2nF (6-inch PDP), $L=L_1=L_2$=73μH, transition time≤800ns, and $M_1$~$M_6$=2SK2995. Fig. 3 shows the experimental results of the proposed circuit. As shown in Fig. 3(a), $C_p$ is fully charged to $V_s$ or $-V_s$ without hard switching due to built-up inductor currents. Moreover, since $i_{L1}$ and $i_{L2}$ compensate for the large amount of the gas-discharge current, the current stress of main switches and voltage notch are effectively reduced. $M_2$ and $M_3$ are turned on under ZVS without severe hard switching due to built-up inductor currents as shown in Fig. 3(b).

## 5. Conclusions

A new low-cost ERC for the PDP has been proposed. The proposed circuit has two auxiliary switches clamped on $V_s/2$, which results in a lower cost of the production compared with prior circuits. Due to the built-up inductor currents, the PDP is fully charged and discharged without hard switching, the ZVS of main switches is achieved, and the EMI noises is reduced. Moreover, since these compensate for a large gas-discharge current, there is no severe voltage notch, and the current stress of main switches can be reduced effectively. The proposed circuit features the high energy-recovery capability. Therefore, it is expected to be suitable for the low-cost PDP.



*(a)* Key waveforms



*(b)* ZVS turn on M2 and M3

Fig. 3 Experimental Results

## References

[1] Weber, L. F., and Wood, M. B.: 'Energy recovery sustain circuit for the AC plasma display', *Proc. S. I. D.*, 1987, pp. 92-95.

[2] Ohba, M., and Sano, Y.: 'Energy recovery driver for a dot matrix AC plasma panel with a parallel resonant circuit allowing power reduction', US Patent 5,670,974, September 1997.