# 새로운 영전압 스위칭 방식을 이용한 고효율 하프-브릿지 컨버터

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# New Zero-Voltage-Switching Method for High Efficiency Half-Bridge Converter

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**ABSTRACT**

This paper proposes a new full ZVS-range asymmetrical half bridge converter. It uses the variable transient current build-up technique with the load variations. The current build-up is accomplished by using the secondary synchronous switch control. Due to the blocking capacitor in secondary side, the voltage applied to leakage inductor varies with the load variations during current build-up period. Therefore, the unnecessary current build-up of leakage inductor current in heavy load condition is prevented and more current build-up in medium and light load condition is achieved for ZVS operation. That is, the variant current build-up with the load variation is accomplished for the ZVS operation. Furthermore, the DC offset of the transformer magnetizing current is also eliminated and the utilization of magnetic core is maximized.

## 1. INTRODUCTION

With the increasing demand for high power density, high efficiency and low cost in the dc/dc converter for the distributed power systems of the server and telecommunication, the switching frequency of converter continues to increase to reduce the size and cost of passive components. With the increased switching frequency, the soft switching operation becomes more desirable to reduce the increased switching losses. Among various soft switching converters, the pulse width modulation asymmetrical half bridge converter with current doubler rectifier (AHBC-CDR) is attractive due to its simple control strategy, zero voltage switching (ZVS) characteristics and smaller passive component size [1-2]. However, since the energy for the ZVS operation is the function of the load current, the ZVS operation of AHBC-CDR is lost in the medium and light load condition. Furthermore, the DC offset of magnetizing current degrades the utilization of magnetic core. To solve these drawbacks, this paper proposes a new variable transient current build-up (VTCB) technique for asymmetrical half bridge converter. Since it controls the secondary synchronous switch to build up the current for the ZVS operation in a very short period of time, the ZVS operation of all power switches is easily achieved through all loads conditions. Furthermore, since the blocking capacitor in the secondary side of transformer prevents the unnecessary build-up of current in the heavy load condition and allows the current build-up as load goes down, the proposed converter makes the variable current build-up condition and different ZVS operation with the load variation. The blocking capacitor also eliminates the DC offset of magnetizing current in the transformer. Therefore, the utilization of magnetic core is maximized. As a results, the proposed converter can achieve high efficiency, high power density and low switching noise throughout all load conditions.

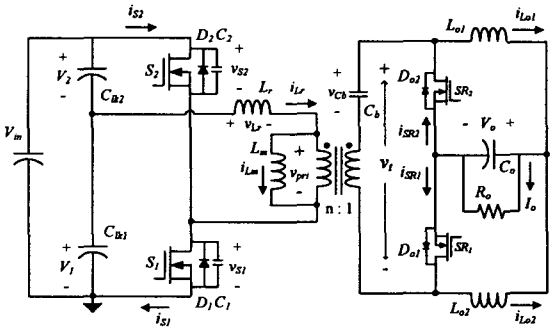

Fig. 1 Circuit diagram of the proposed converter

## 2. OPERATIONAL PRINCIPLE

The circuit configuration of the proposed converter is the same as that of the conventional half bridge converter with current doubler rectifier except for the added blocking capacitor $C_b$ in the secondary side of transformer as shown in Fig. 1. $S_1$ is operated in duty ratio of D, and $S_2$ is operated with complementary to $S_1$ with the time delay between their gate pulses. Fig. 2 shows the gating pulses for switches and key

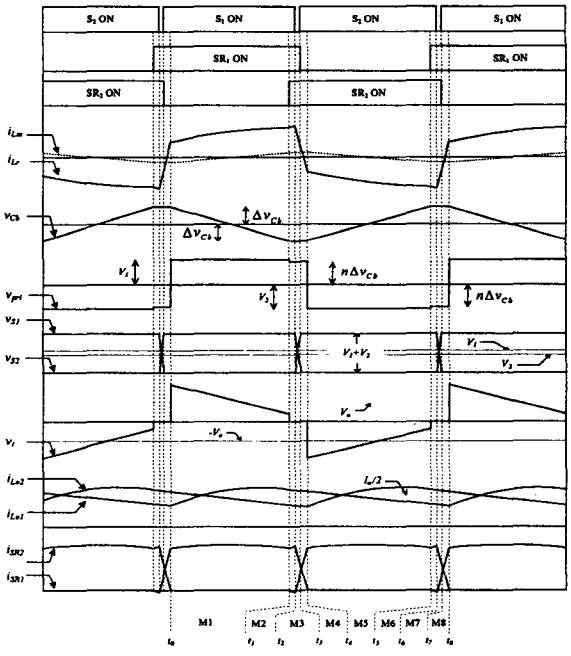

Fig. 2 Key waveforms for the mode analysis

operating waveforms of the proposed converter in the steady state. The gating pulses for $SR_1$ and $SR_2$ are imposed before $S_2$ and $S_1$ are turned off, respectively. One switching cycle is divided into two half cycles, $t_0$~$t_4$ and $t_4$~$t_8$, and only the first half cycle is explained. M

***Mode 1($t_0$~$t_1$):*** Mode 1 begins at $t_0$ when the commutation of $i_{SR1}(t)$ and $i_{SR2}(t)$ is completed. Then, $i_{Lo2}(t)$ flows through $C_o$ and $SR_1$. And, $i_{Lo1}(t)$ flows through $C_o$, $SR_1$ and $C_b$. Therefore, $v_{Cb}(t)$ is linearly decreased as time goes by in this mode. The increasing slope of $i_{Lo1}(t)$ and $i_{Lr}(t)$ is decreased in Fig. 2 due to the decrease of $v_{Cb}(t)$ in this mode. This mode ends when the gating pulse of $SR_2$ is imposed while $S_1$ and $SR_1$ are still on state.

***Mode 2($t_1$~$t_2$):*** Since $SR_2$ is turned on while $SR_1$ is on state, the voltage across secondary winding becomes $\Delta v_{Cb}$, and $v_{pri}(t)$ becomes $n\Delta v_{Cb}$ as shown in Fig. 2. And, since $S_1$ is also on state, $V_1$-$n\Delta v_{Cb}$ is applied to $L_r$. Therefore, the current build-up in $L_r$ occurs as can be seen in $i_{Lr}(t)$ waveform of Fig.2. This build-up current is used for the ZVS operation of $S_2$ in mode 3.

***Mode 3($t_2$~$t_3$):*** Mode 3 begins when $S_1$ is turned off at $t_2$. Then, the resonance between $L_r$ and $C_1$+$C_2$=$2C_s$ occurs and the output capacitor of $S_1$ and $S_2$ is charged and discharged by leakage inductor current, respectively.

***Mode 4($t_3$~$t_4$):*** Mode 4 begins when the voltage of $S_2$ decreases to zero and the switch $S_2$ is turned on. This mode ends when the communication of $i_{SR1}(t)$ and $i_{SR2}(t)$ is finished at $t_4$. The circuit operation of $t_4$~$t_8$ is similar to that of $t_0$~$t_4$. Subsequently, the operation form $t_0$ to $t_8$ is repeated.

## 3. ANALYSIS OF THE PROPOSED CONVERTER

### *A. ZVS analysis with the load variation*

In conventional AHBC-DCR, the ZVS operation is the function of load current. That is, the ZVS operation is easily achieved in heavy load condition by the reflected large load current. However, as load goes down, the reflected load current is also reduced and finally the ZVS operation is not guaranteed. To solve these problems, large leakage inductor is necessary or large magnetizing current is required by reducing the magnetizing inductance of transformer. However, these methods cause lots of problems such as reduced effective duty, large oscillation of output rectifier's voltage and additional conduction loss and core loss of transformer. In the proposed converter, since the current of leakage inductor is built up in a very short period of mode 2 and mode 6, large leakage inductor or large magnetizing current are not necessary to achieve the ZVS operation of power switches. Therefore, it can solve the problems mentioned above. If the blocking capacitor $C_b$ does not exist in the proposed converter, the current is built up regardless of load condition in mode 2 and mode 6. However, since the ZVS operation is easily achieved by the reflected large load current in heavy load condition, the build-up of current for the ZVS operation is not necessary. Therefore, the blocking capacitor $C_b$ is adapted in the proposed converter. Fig. 3 shows the voltage of $C_b$, the voltage across $L_r$ and the current of $L_r$ according to the load variation. The decrease of duty ratio by the parasitic component with the load variation is ignored for the convenience of analysis in Fig. 3. The peak voltage of $v_{Cb}(t)$ is defined as $\Delta v_{Cb1}$ and $\Delta v_{Cb2}$ in heavy load and light load condition, respectively. Since the current flows through $C_b$ is decrease as load goes down, $\Delta v_{Cb2}$ in much smaller than $\Delta v_{Cb1}$. In mode 2, $SR_2$ is turned on while $S_1$ and $SR_1$ are on state. Then, the voltage $V_1$-$n\Delta v_{Cb1}$ is applied to leakage inductor as shown in Fig. 3(a). Since the voltage $n\Delta v_{Cb1}$ is almost the same as $V_1$, the voltage $V_1$-$n\Delta v_{Cb1}$ is very small. Therefore, the leakage inductor current is barely built up in heavy load condition. However, as load goes down, the peak value of $v_{Cb}(t)$ decreases and finally reaches to $\Delta v_{Cb2}$ in the light load condition. Since the voltage $\Delta v_{Cb2}$ is much smaller than $V_1$, the large voltage $V_1$-$n\Delta v_{Cb2}$ is applied to leakage inductor in mode 2 of Fig. 3(b). Therefore, the larger leakage inductor current is built up, and this build-up current helps the ZVS operation of $S_2$ in the light load condition in mode 3. By adapting the current build-up technique and the blocking capacitor in the secondary side of transformer, the proposed converter shows the different current build-up condition and different ZVS operation with the load variation. Therefore, the considerably effective ZVS characteristics in the full load ranges can be ensured without any additional losses. The ZVS operation of $S_1$ is symmetrical to $S_2$.

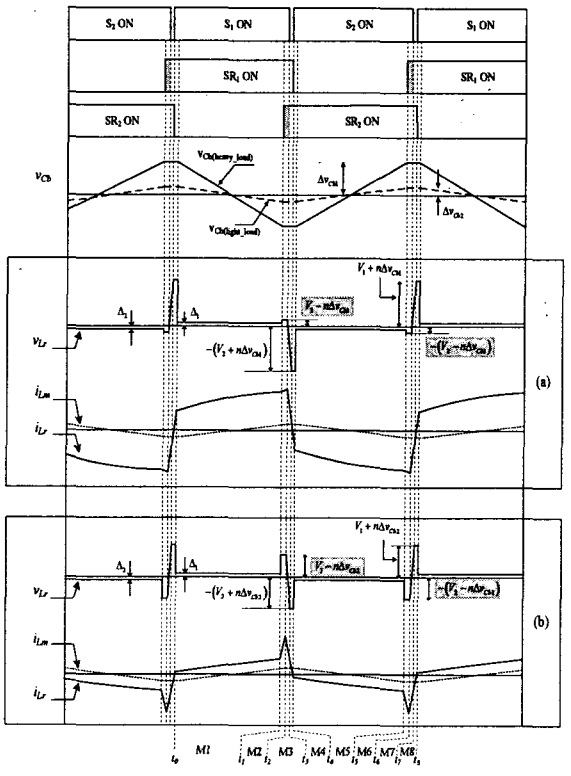


Fig. 3 ZVS operation with the load variation

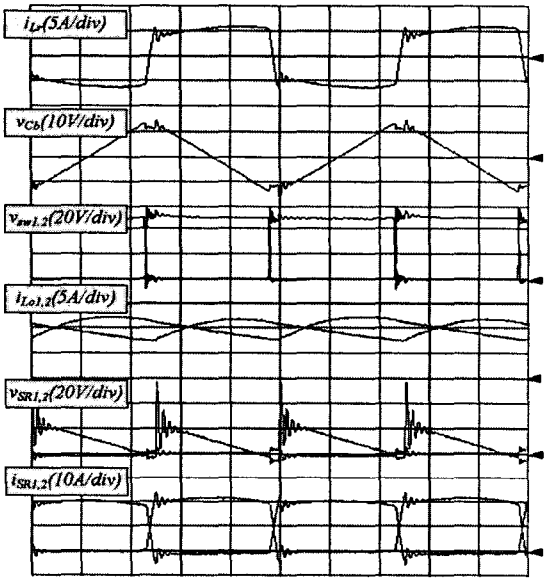


Fig. 4 Key experimental waveforms at full load condition

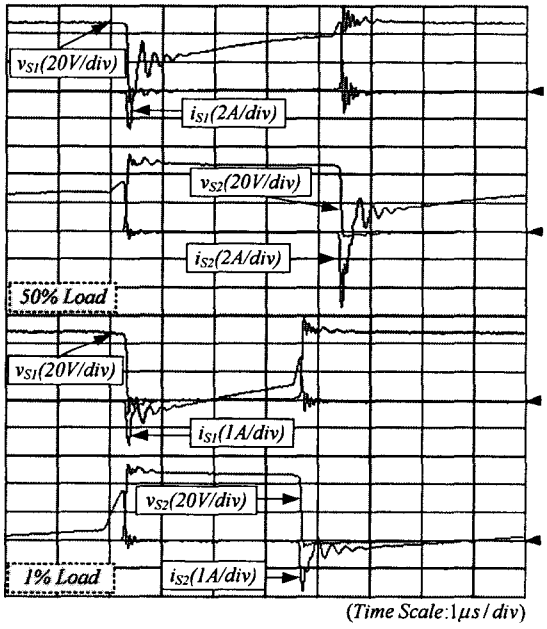


Fig. 5 ZVS waveforms with the load variation

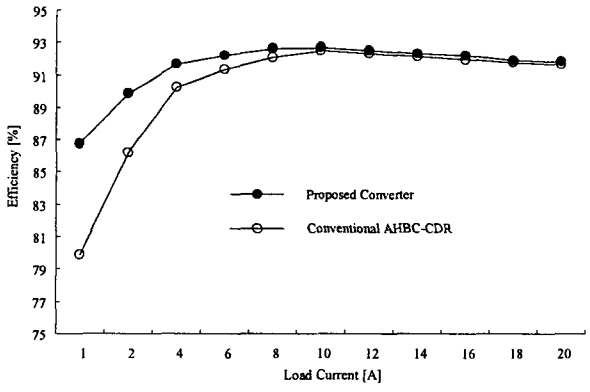


Fig. 6 Efficiency comparison with the load variation

*B. Zero DC offset of transformer magnetizing current*

In the conventional AHBC-CDR, the DC offset of transformer magnetizing current is the function of duty ratio, load current and DC resistance of transformer and output inductors. Thus, the transformer should have the air gap to prevent the saturation of the core [3]. This causes additional core and conduction losses and reduces the power density of the converter. However, in the proposed converter, the blocking capacitor $C_b$ eliminates the DC offset of the transformer magnetizing current. From Fig. 1 the leakage inductor current can be expressed as $i_{Lr}(t)=i_{Lm}(t)+i_{pri}(t)$ and the DC value of that can be expressed as $i_{Lr(DC)}=i_{Lm(DC)}+i_{pri(DC)}$. Since the DC value of the current flows through the capacitor $i_{Cb(DC)}$ is 0A in steady state, $i_{pri(DC)}=0A$. Applying the current-second balance of to link capacitor $C_{lk1}$, $i_{Lr(DC)}$ is also derived to 0A. Since $i_{Lr(DC)}=i_{pri(DC)}=0A$, the DC value of transformer magnetizing current becomes zero. Therefore, the transformer magnetic core can be fully utilized.

## 4. Experimental Results and Conclusion

A prototype of a 5V, 100W converter is constructed. Fig. 4 shows key waveforms of the proposed converter at full load condition. Since the peak value of $v_{Cb}(t)$ is almost the same as $V_1/n$, there is no current build-up in $i_{Lr}(t)$ waveform. The ZVS operation of switch $S_1$ and $S_2$ is easily achieved by the large load current and the ripple of output inductor current is almost 4A. Due to the effect of the blocking capacitor, the current slopes of $i_{Lo1}(t)$ and $i_{Lo2}(t)$ are varying during $DT_s$ and $(1-D)T_s$, respectively. As shown in Fig. 5, the ZVS operation of proposed converter is achieved form full load to very light load condition. Fig. 6 shows the efficiency curves of proposed converter and conventional AHBC-CDR with the load variation. In heavy load condition, since the proposed converter doesn't require air gap in the transformer, more magnetizing inductance and less magnetizing current is used. This results in higher efficiency than that of conventional one. It also shows greatly higher efficiency than conventional one in the light load condition due to the proposed current build-up ZVS technique. By using the current build-up technique and the different ZVS operation with the load variations, the proposed converter does not cause additional losses in heavy load condition and can guarantees ZVS operation throughout full load ranges.

## References

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