A New Planar Spiral Inductor with Multi-layered Bragg Reflector for Si-Based RF IC's

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ABSTRACT

In this paper, a novel physical structure for planar spiral inductors is proposed. The spiral inductors were designed and fabricated on multi-layered substrate Bragg-reflector/silicon (BR/Si) wafer. The impacts of multi-layered structure substrate and pattern on characteristics of inductor were studied. Experimental results show that the inductor embedded on Bragg reflector/silicon substrate can achieve the best improvement. At 0.4 - 1.6 GHz, the Bragg reflector seems to significantly increase the S_{11}-parameter of the inductor.

Keywords

Inductor, Bragg reflector, substrate loss, return loss S_{11}.

I . Introduction

Nowadays, the wireless communication circuits need to have low supply voltage, low power dissipation, low noise, high frequency of operation and low distortion. These requirements for high performance RF circuits cannot be met easily in many cases without the use of inductors, especially on-chip spiral inductors. Typical applications of the on-chip spiral inductors include low loss inductor for input matching of low noise amplifiers, inductively loaded pre-amplifiers output matching networks for high efficiency power amplifiers, and high-Q tank circuits for low phase noise voltage control oscillators. Many researches have been reported on the on-chip spiral inductors' physical structure design and modeling. A new physical structure for on-chip spiral inductor leads to new prospects of RF ICs fabrication in wireless communications.

Conventionally, RF micro-inductors have been fabricated on the planar substrates such as silicon or glass [1-3]. The losses caused by conductive substrates and thin metal strips are main drawbacks in improving the performance of those planar inductors. In order to improve the performance of on-chip spiral inductor, many methods have been used to decrease the substrate loss and ohmic loss. Larson [4] employed thick dielectric layers to reduce the substrate loss and use higher conductivity metal such as gold to lower the resistance loss of spiral inductors. Taub et al.[5] proposed high resistive silicon or silicon-on-insulator as the substrate. Another method to reduce substrate loss is the removal of the conductive substrate [6, 7]. However, the high Q-value of on-chip spiral inductors achieved by those conventional/unconventional methods suffers from the cost of complex process and different technology or, together with decreasing the mechanical strength. Thus, they seem somewhat not easy for fabrication and commercialization.

In this work, we, for the first time, proposed and implemented a new physical structure of on-chip spiral inductors incorporating Bragg reflector multi-layered between the spiral and silicon wafer. Thus, the substrate loss can be reduced, and the inductor performance can be improved.

II. Experiment

Three sets of different spiral inductors (I1, I2, and I3) are simultaneously prepared on three different silicon-based substrates Si, SiO_2/Si, and BR/Si, respectively.

Fig. 1 illustrates different inductor structures considered in this work: (a) inductor on silicon substrate; (b) inductor on SiO_2/Si substrate; (c) inductor on BR 7-layered/Si substrate.

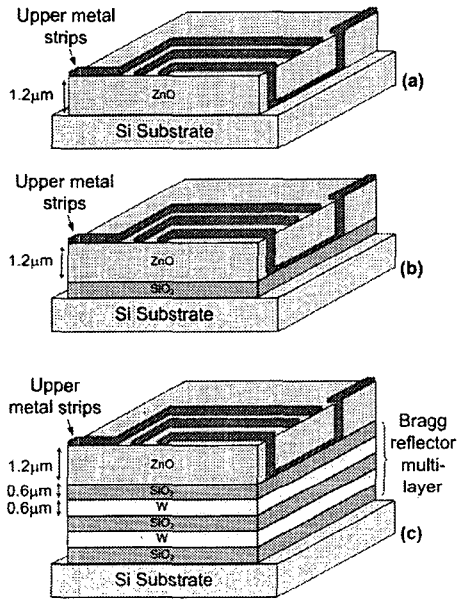

Fig. 1 Cross-section 3-D structure of on-chip inductor (a) Inductor on Si substrate
(b) Inductor on SiO_2/Si substrate
(c) Inductor on BR/Si substrate

The first spiral type I1 was fabricated directly on Si wafer in order to use it as a reference sample. The second type of spiral I2 was fabricated similar to the first one but the spiral inductors were separated from the Si wafer by 0.6 μm of thermal silicon dioxide (SiO_2). The last inductor type I3 - our proposal - was fabricated on the multi-layered Bragg reflector/silicon substrate (BR/Si). The multi-layered Bragg reflector has seven layers of SiO_2 and tungsten (W) films deposited alternately by using an RF magnetron sputtering technique. The 0.6 μm thick W films were deposited under Ar gas pressure of 15 mTorr with DC power of 150 Watts, and the 0.6 μm thick SiO_2 films were deposited under Ar gas pressure of 4 mTorr with RF power of 300 Watts. Each spiral was fabricated using 0.2 μm thick aluminum (Al) with 1.2 μm thick zinc oxide (ZnO). The 0.2 μm thick Al thin films (lower metal strips) were simultaneously deposited on all three substrates under 20 mTorr Ar gas pressure and with 150 Watts DC power. Then, 1.2 μm thick ZnO film with via-patterning was deposited under 10 mTorr of Ar/O_2 mixed-gases, and with RF power of 300 Watts. The deposition and patterning of the upper Al strips (0.2 μm) on top of the ZnO film completed the spiral inductor fabrication. All the upper metal strips are connected with the lower ones through via-holes. Finally, the three spiral inductor types (I1, I2, and I3), each corresponding to the substrates of Si, SiO_2/Si and BR/Si, were obtained. All spiral were measured to extract the de-embedded S-parameters using probe station and network analyzer Hewlet Packard/HP 8722D.

III. Results and discussion

In this paper, three types of spiral inductor layouts were designed and each one was fabricated on three different substrates structures, as described in Fig. 1 of the section 2. The measured S-parameter of three inductor patterns as a function of frequency is shown in Fig. 2. The three spiral patterns have 2.5 turns and number of sides is 12, 14, and 16, respectively. Fig. 2 (a), (b), (c) compare the return loss characteristics of the 3 spiral inductor structures (namely L1, L2, and L3) with the same inductor layout, each fabricated on the Si, SiO_2/Si, and BR/Si substrates, respectively. The comparison of the S_{11} values clearly shows the relative effect of the substrate structure used. Regardless of the spiral inductor layout types, the return loss values have the same increasing trend in sequence from the inductor L1 (Si substrate), the inductor L2 (SiO_2/Si substrate), and the last one L3 (BR/Si substrate). For three physical inductor structures, the S_{11} characteristic of inductor L2 is better than of L1 due to the dielectric layer SiO_2 incorporated between spiral inductor and Si substrate for the reduction of the substrate loss. Meanwhile, the return loss S_{11} value of inductor L3 is significantly improved when

compare with the other inductors L1 and L2. The return loss S_{11} value seems to be much improved since the inductors were fabricated farther away the silicon substrate with multi-layered Bragg reflector.

Undoubtedly, the employing seven-layered Bragg reflector can reduce the loss of Si substrate more effectively. Therefore, the BR/Si substrate can act a reflected-substrate underneath the inductor, eventually increasing resistivity of Si substrate and thus decreasing harmful parasitic components between metal strips and Si substrate. As a result, the substrate effects of spiral inductors are suppressed. From the measured S-parameters, these inductors can be used in the frequency range from 0.4-1.6 GHz. As shown in Fig. 2, when frequency increases to 1.6 GHz, S_{11} parameters reduce to zero due to the self-resonance frequency. Although further investigations need to be done for more clear understanding, we strongly believe at this point that the use of Bragg reflector can significantly improve the on-chip inductor performance. And the new physical structure of planar inductor seems highly feasible for the Si-based process RF IC applications.

IV. Conclusion

A novel spiral inductor fabricated on a multi-layered Bragg reflector is proposed. The multi-layered Bragg reflector was deposited on a Si substrate. The spiral inductor with Bragg reflector multi-layered has shown better performance than other conventional spiral inductors. This new inductor design seems very promising for the future Si-based RFIC fabrications.

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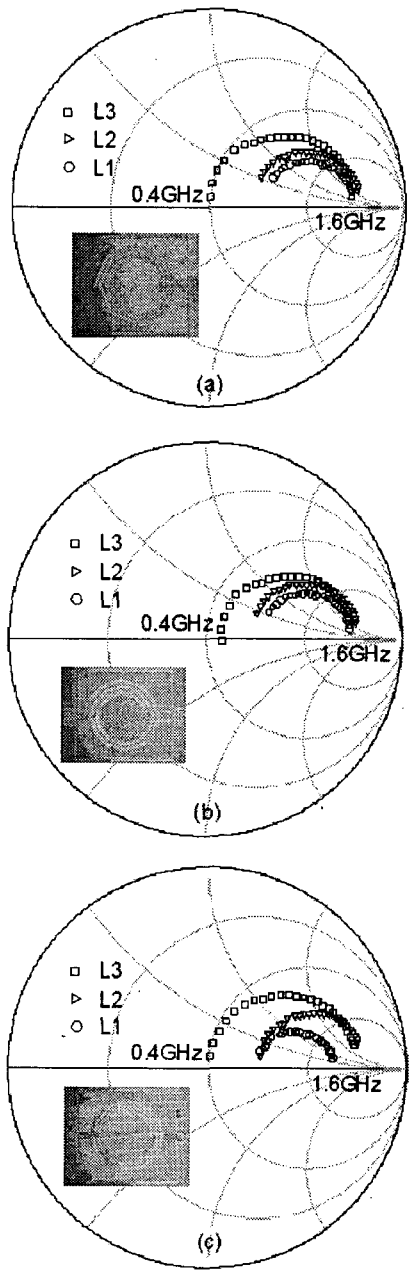

Fig. 2 Measured values of return loss S_{11} from 0.4 - 1.6 GHz plotted on a Smith chart for 3 different types of spiral inductor structures. (a) spiral layout L1 (b) spiral layout L2 (c) spiral layout L3

REFERENCE

[1] C.P. Yue, S.S. Wong, Physical modeling of spiral inductors on silicon, IEEE Trans. Electron Devices, 47 (2000), 560-568.

[2] C.J. Chao, S.C.Wong, C.H.Kao, M.J. Chen, Characterization and modeling of on-chip spiral inductors for Si RF ICs, IEEE Trans. on Semiconductor Manufacturing 15 (2002), 19-29.

[3] J.N. Burghartz, D.C. Edelstein, M. Soyuer, H.A. Ainspan, K.A. Jenkin, RF circuit design aspects of spiral inductors on silicon, IEEE Journal of Solid-State Circuits 33 (1998), 2028-2034.

[4] L.E. Larson, Integrated circuit technology options for RF ICs present status and future directions, IEEE Journal of Solid-State Circuits 33 (1998), 387-399.

[5] S.R. Taub, S.A. Alterovitz, Silicon technologies adjust to RF applications, Microwave and RF (1994), 60-74.

[6] X.-N. Wang, X.-L. Zhao, Y. Zhou, X.-H.. Dai, B.-C. Cai, Fabrication and performance of novel RF spiral inductors on silicon, Elsevier Microelectronics Journal (2004), 1-4.

[7] K.C. Eun, C.S. Park, Air cavity incorporation to LTCC spiral inductor for high Q-factor and SRF, Elsevier International Journal (AEU) of Electronics and Communications Letter (2003), 434-436.