

ZnO/GaN 이종접합구조의 capacitance-voltage 특성에 관한 연구

오동철, 한창석, 구경완, 정돈원*
호서대학교 국방과학기술학과, 영동대학교 컴퓨터공학과*

Capacitance-voltage characteristics of ZnO/GaN heterostructures

Dong-Cheol Oh, Chang-Suk Han, Kyung-Wan Koo, Soon-Won Jung*
Department of Defense Science & Technology, Hoseo University
Department of Computer Engineering, Youngdong University*

Abstract : Capacitance-voltage(C-V) 측정평가를 통하여 ZnO/GaN 이종접합구조의 전기적인 특성을 조사한다. 실온에서 10kHz의 주파수에서 얻은 ZnO/GaN의 이종접합구조에 대한 C-V 측정결과는 이종접합계면에서 고밀도의 전자가 축적되어 있음을 나타낸다. 이것은 ZnO/GaN 이종접합계면의 다른 재료에서 볼 수 없는 큰 전도대불연속에 기인한 것인데, 각각의 층의 전도도를 제어함으로써 이종접합계면에 축적되는 전자밀도를 $\sim 10^{19}\text{cm}^{-3}$ 까지 증가시킬 수 있다. 따라서 ZnO/GaN 이종접합구조는 이종접합트랜지스터로서 유망한 재료로 판단된다.

Key Words : ZnO, ZnO/GaN heterostructure, capacitance-voltage characteristics

1. Introduction

ZnO with a wide bandgap of 3.4 eV is well known as a promising material for light-emitting devices in blue and ultraviolet (UV) regions, because of the large exciton binding energy of 60 meV - 3 times large than 21 meV in GaN [1].

ZnO/GaN heterostructures are very attractive as heterojunction devices, because a large bandgap discontinuity at heterointerface is expected. Johnson et al. have reported that the valence band of GaN is estimated to be located at 0.6 eV above the valence band of ZnO based on the electron affinity rule [2]. Hong et al. have by using X-ray photoelectron spectroscopy observed that the ZnO/GaN hetero-interface is made up of the type II band alignment with the valence-band offset of 0.8 eV [3]. Moreover, ZnO/GaN heterostructures also have attractive merits in the aspect of crystal growth. GaN is good choice for a template for ZnO growth, because ZnO is a closely lattice-matched material to GaN with a lattice mismatch of 1.8 % [4], which is ten times smaller than Al_2O_3 that is normally used as a substrate for ZnO. In the case that GaN with Ga polarity is used as a template, the polarity of ZnO can also be easily controlled by changing pre-exposure conditions [5].

However, the studies for the electrical properties of ZnO/GaN heterointerface are still lack [6]. These are ascribed to the conducting layers at ZnO surface that

hampers the fabrication of good Schottky contact to ZnO and restricts the electrical characterization of interface or bulk. In this work, we evaluate the capacitance -voltage (C-V) characteristics for ZnO layers grown on GaN templates in terms of fabricating Schottky contacts using Schottky barrier layers of heavily doped ZnO:N layers.

2. Experiment

ZnO layers were grown on Ga-polar GaN templates by plasma-assisted molecular-beam epitaxy (P-MBE), equipped with a Zn solid source, an O rf-plasma source, and a N rf-plasma source. The GaN template used in this work was predeposited by metal-organic chemical-vapor deposition (MOCVD) on a (0001) Al_2O_3 substrate and n-type with an electron concentration of $2 \times 10^{18}\text{cm}^{-3}$. First, a low-temperature ZnO buffer at 500°C was grown on the GaN template, followed by high-temperature annealing at 800°C . Subsequently, a ZnO layer was grown at 700°C . Finally, a ZnO:N capping layer was grown at 300°C for the formation of Schottky contact. Then, the thickness of ZnO and ZnO:N layers were 1000 nm and 10 nm, respectively. In fabricating Schottky barrier diodes, Au electrodes ($\sim 5\text{nm}$) were deposited on ZnO surfaces for Schottky contact and In electrodes were deposited on GaN surfaces after etching out ZnO:N and ZnO layers for Ohmic contact. Then, the Au Schottky electrode had a diameter of 1 mm and the sample size was 5 mm by 10

mm. The electrodes were evaporated in a vacuum chamber, immediately after organic cleaning, in order to remove contaminants from sample surface.

3. Results and discussion

Figure 1 shows the depth profile of electron concentration for the ZnO/GaN heterostructures, obtained at 10 kHz and room temperature. The depth profile shows that electron concentration decreases, increases, and decreases as the depth is farther from the ZnO surface. The first region of decreasing electron concentration is caused by the carrier depletion due to the Schottky barrier of Au/ZnO:N/ZnO [6-9]. Then electron concentration increases rapidly up to $\sim 10^{18}$ cm⁻³ at the ZnO/GaN heterointerface. We note that ZnO becomes electrically degenerate at an electron concentration of 4.5×10^{18} cm⁻³. The large density of negative charges accumulated at the ZnO/GaN interface is due to the large conduction-band discontinuity and gives rise to the large plateau region observed in the C-V curves [6-9]. The build-up of electron concentration at the ZnO/GaN heterointerface is comparable to 3×10^{17} cm⁻³ at Al_{0.3}Ga_{0.7}As/GaAs and 3×10^{17} cm⁻³ at In_{0.5}Ga_{0.5}P/GaAs [6-9]. Recently, Hong et al. have experimentally shown that the ZnO/GaN heterointerface is made up of the type II alignment with the valence-band offset of 0.8 eV i.e., the conduction-band offset of the ZnO/GaN heterointerface is 0.82 eV, which is more than 2.5 times larger than those at Al_{0.3}Ga_{0.7}As/GaAs

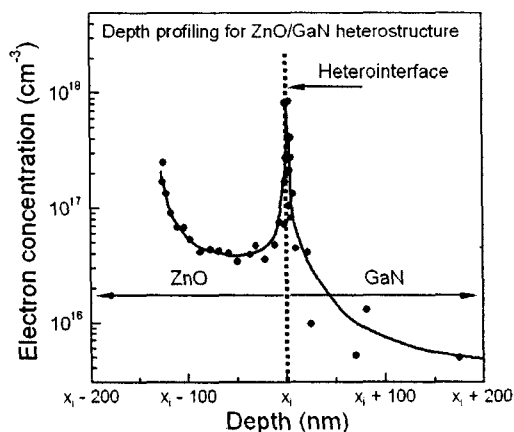


Fig. 1. Depth profile of electron concentration at ZnO/GaN heterostructures at 10 kHz and room temperature

and Al_{0.15}Ga_{0.85}N/GaN heterointerfaces [6-9]. Finally, the rapid increase of electron concentration is followed by the drastic decrease of carrier concentration down to below 1×10^{16} cm⁻³, two orders lower than its bulk concentration 2×10^{18} cm⁻³. This phenomenon is ascribed to the carrier depletion in underlying GaN [6-9]. Such carrier depletion at the ZnO/GaN heterointerface has been commonly found in inverted structures (i.e. narrow-bandgap on wide-bandgap heterojunctions).

4. Conclusions

We investigated the electrical properties of ZnO/GaN heterointerface using C-V measurements.

ZnO/GaN heterostructures exhibited a large electron density of $\sim 10^{18}$ cm⁻³ at the heterointerface in depth profile. It is ascribed to the large conduction-band discontinuity at ZnO/GaN heterointerface. The value is comparable to the reported values in other hetero-structures. Consequently, it is suggested that the ZnO/GaN heterostructure is a very promising material for the application of heterojunction transistors.

References

- [1] D. C. Look, *Mat. Sci. Eng. B* **B80**, 383 (2001).
- [2] M. A. L. Johnson, S. Fujita, W. H. Rowland, Jr., W. C. Hughes, J. W. Cook, Jr., and J. F. Schetzina, *J. Electron. Mater.* **25**, 855 (1996).
- [3] S. K. Hong, T. Hanada, H. Makino, Y. Chen, H. J. Ko, T. Yao, A. Tanaka, H. Sasaki, and S. Sato, *Appl. Phys. Lett.* **78**, 3349 (2001).
- [4] H. J. Ko, Y. F. Chen, T. Yao, K. Miyajima, A. Yamamoto, and T. Goto, *Appl. Phys. Lett.* **77**, 537 (2000).
- [5] S. K. Hong, T. Hanada, H. J. Ko, Y. Chen, T. Yao, D. Imai, K. Araki, and M. Shinohara, *Appl. Phys. Lett.* **77**, 3571 (2000).
- [6] B. J. Coppa, R. F. Davis, and R. J. Nemanich, *Appl. Phys. Lett.* **82**, 400 (2003).
- [7] M. A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, *IEEE Electron Device Lett.* **21**, 63 (2000).
- [8] M. O. Watanabe, J. Yoshida, M. Mashita, T. Nakanisi, and A. Hojo, *J. Appl. Phys.* **57**, 5340 (1985).
- [9] M. O. Watanabe and Y. Ohba, *Appl. Phys. Lett.* **50**, 906 (1987).