SPICE Modeling of Organic Field Effect Transistors (OFETs)

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유기 박막 트랜지스터의 스파이스 모형화

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Abstract: Organic thin film transistors(OTFTs) were simulated by a SPICE model adopted in the amorphous TFTs(a-Si:H TFTs). The gate voltage-dependent mobilities were assumed to fit the representative current-voltage characteristics. The optimal fitting procedures were suggested to compare the experimental data with the mathematical expressions used in the amorphous TFTs. Each SPICE parameter explains the gate dependent mobilities in OTFTs which might originate from the influence of the hopping conduction.

Key Words: SPICE, OTFTs, Parameters

1. Introduction

performance of Organic Thin As the Transistors(OTFTs) has substantially improved, it is expected that they will be more widely used as practical devices. Modeling of OTFTs by circuit simulation tools such as SPICE is needed so that OTFTs could be properly applied to the integrated circuit electronics. Although the electrical transport characteristics are not fully understood, it is generally accepted that the model used for hydrogenated amorphous silicon(a-Si:H) transistors could be employed. For explaining the case of OTFTs, one of the reason why this model could be used is that the low conductivity of both of these materials is due to large concentrations of traps that limit the charge-carrier transport[1]. However, a disadvantage of this model is that there are so many empirical parameters that extracting parameters is not straightforward. An useful method for extracting parameters from the current-voltage measurements is suggested.

2. Parameter Extraction Method

The mobility with a semi-empirical gate-voltage dependence in the trapping model mentioned above is expressed as following eq. (1)[2].

$$\mu = \kappa (V_G - V_T)^{\gamma} \qquad \dots (1)$$

Applying the gradual channel approximation, the drain-source current I_d in the linear regime where the drain-source voltage is kept small is denoted:

$$I_{d} = \frac{W}{L} C_{i} \mu [(V_{G} - V_{T})] V_{D} \qquad ...(2)$$

In the linear regime, the channel conductance g_d is simply

 I_d divided by the constant V_d [3]:

$$g_{d} = \frac{\partial I_{d}}{\partial V_{D}} = \frac{I_{d}}{V_{D}} = \left(\frac{1}{(W/L)C_{i}\mu(V_{G} - V_{T})} + R_{S}\right)^{-1}$$

$$= \left(\frac{1}{(W/L)C_{i}\kappa(V_{G} - V_{T})^{\gamma+1}} + R_{S}\right)^{-1} \qquad ...(3)$$

Assuming the mobility is dependent on the gate voltage, the mobility will change along the channel as the effective gate voltage is varied between the drain region and the source region with the non zero drain source bias. Therefore, one of the methods to estimate the gate-voltage dependent mobility is to apply the lowest possible drain-source voltage and carry out the measurements so that the mobility remains practically constant all along the conducting channel [3].

The nonlinear fitting was done from the transfer curve at a linear regime with V_{ds} =-6V to extract parameters from the experimental results found in the Reference [4].

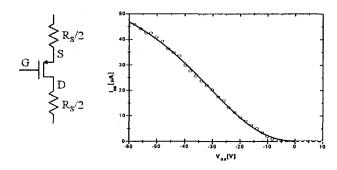


Figure 1. Equivalent circuit diagram (left) and the fitted result of the data according to Eq. (3) (right)

The amorphous silicon TFT model in AIM-SPICE(ASIA2, Level 15) was used, and the expression for the current given as following eq. (4) [5,6]:

$$I_{d} = \frac{K/V_{dd}^{T}}{1 + R_{s}(K/V_{dA}^{T})(V_{G} - V_{T})^{1+T}} \times \frac{(V_{G} - V_{T})^{1+T}V_{D}(1 + \lambda V_{D})}{\left[1 + \left[\frac{V_{D}}{V_{Diat}}\right]^{M}\right]^{1/M}} \dots (4)$$

Based on the parameters acquired as above at the linear reigme(γ, V_{AA}, V_T, R_S), the rest three parameters(M, λ, α_{SAT}) were varied simultaneously and the differences between the calculated currents and the measured values were compared.

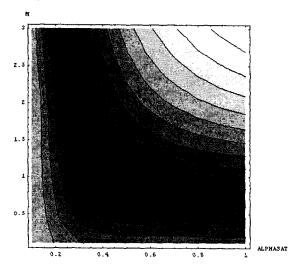


Figure 2. Contour plot of Fig 2. with the variation of the parameters (α_{SAT}, M)

In the 3D graph, the spatial coordinates correspond to the combinations of three simulation parameters (λ , α_{SAT} , M) and the color indicates the difference between calculated values and measured values representing the darker for the smaller difference. The final set of the parameters are given to the SPICE simulator and the simulated results are compared with the measurements.

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Figure 3. The set of parameters used in the SPICE simulation (top), the experimental data and fitted results according to Eq. (4) (left) and fitting parameters (right)

3. Conclusion

Parameters used in modeling OTFTs were extracted from the current-voltage measurements of real devices. Simulation results with the extracted parameters were fitted relatively well with measurements. However, the parasitic resistance between the drain/source region and conducting channel resulted in one or two orders of the excess currents. The parasitic resistance was suggested to depend on not only the gate voltage but also the drain-source voltage.

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