Study of thermal stability of Ni Silicide using Ni-V Alloy

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Abstract : In this paper, Ni-V alloy was studied with different structures and thickness. In case of Ni-V and Ni-V/Co/TiN, low resistive Ni silicide was formed after one step RTP (Rapid Thermal Process) with temperature range from 400℃ to 600℃ for 30sec in vacuum. After furnace annealing with temperatures range from 550℃ to 650℃ for 30min in nitrogen ambient, Ni-V single structure shows the best thermal stability compare with the other ones. To enhance the thermal stability up to 650oC and find the optimal thickness of Ni silicide, different thickness of Ni-V was studied in this work. Stable sheet resistance was obtained through Ni-V single structure with optimal Ni-V thickness.

Key Words : Ni-V(Nickel vanadium), thermal stability, Ni silicide, RTP

1. Introduction

Self-aligned silicide (Salicide) is one of key issues in modern ULSI technologies. Recently, Ni silicide (NiSi) has received much attention because of its low resistivity, low formation temperature, small stress and less silicon consumption as compared with the commonly used silicides: TiSi2 and CoSi2 [1-3]. However, Ni silicide has poor thermal stability which because of the formation of high-resistivity phase NiSi2. To improve the thermal stability, many trials such as ion implantation [4], alloy target of NiTa [5], NiPd [6] and multi layer have been performed.

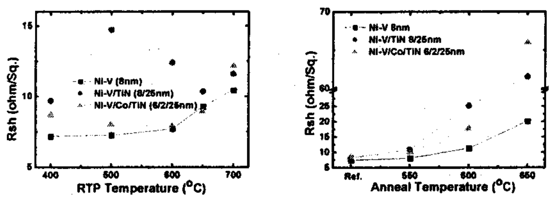
In this paper, different structures include Ni-V, Ni-V/TiN and Ni-V/Co/TiN was investigated to enhance the thermal stability of Ni silicide. Ni-V indicated better thermal stability characteristic in comparison with Ni-V/TiN and Ni-V/Co/TiN. Moreover, in case of Ni-V, the more thickness was deposited, the more stable it shows.

2. Experiment

For experiments, Ni-V, Co and TiN layers were deposited on the p-type Si wafer using RF magnetron sputtering system with Ar ambient. The film structures used in this experiment are (1) Ni-V (8nm,10nm,15nm), (2) Ni-V/TiN (8nm/25nm), (3) Ni-V/Co/TiN (6nm/2nm/25nm). Nickel silicide was formed by rapid thermal process (RTP) at five different temperatures (400 , 500, 600, 650 and 700℃) for 30sec. To test the thermal stability, samples were furnace annealed in three different temperatures (550, 600 and 65 0℃) for 30min. Sheet resistance was measured using conventional four point probe (FPP), AFM (Atomic Force Microscope) analysis was performed to investigate surface roughness and silicide phase identification. Profile of Nickel silicide was characterized by FE-SEM(Field Emission Scanning Electron Microscopy).

3. Results and Discussion

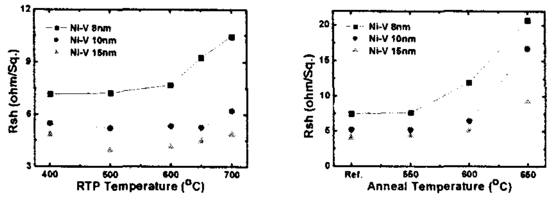
Fig. 1(a) shows the sheet resistance of nickel silicide as a function of the formation temperature. It can be seen that Ni-V structure shows lower sheet resistance compare with the other structures we studied in this experiment. Moreover, after furnace annealing for 30 min with three different temperatures, nickel silicide formed with Ni-V system shows better thermal stability than that formed with Ni-V/Tin and Ni-V/Co/TiN structures as shown in Fig. 1(b). Sheet resistance of nickel silicide showed drastic increase from annealing temperature at 600℃, it was main because of the formation of agglomeration and transition from low-resistivity phase mono-silicide (NiSi) to high-resistivity phase di-silicide (NiSi2).



(a) (b)

Fig. 1 Sheet resistance of Nickel silicide (a) after RTP and (b) after furnace annealing.

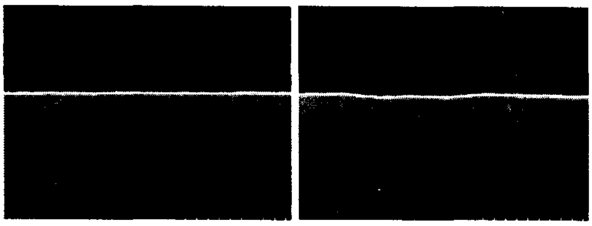
Fig. 2 shows the thermal stability of Nickel silicide dependent on the thickness of Ni-V in case of Ni-V system. As you see, it shows better thermal stability as the increase of thickness of Ni-V. The sheet resistance of Nickel silicide with 8nm Ni-V increased over to 10 Ohm/Sq. only at the annealing temperature of 600℃ while 15nm Ni-V maintained its low and stable sheet resistance up to 600℃.



(a) (b)

Fig. 2 Sheet resistance of Nickel silicide in Ni-V system (a) after RTP and (b) after furnace annealing.

Cross-sectional FE-SEM images of nickel silicide after post-silicidation annealing were shown in Fig. 3. Ni-V/TiN and Ni-V/Co/TiN all showed agglomeration after annealing at 650℃ which can explain the drastic increase of sheet resistance at annealing temperature at 650℃ as shown in Fig. 1(b). Contrary to these cases, Ni-V shows better silicide/silicon interface profile.

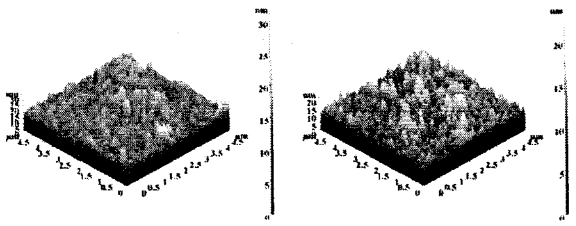


(a) (b)

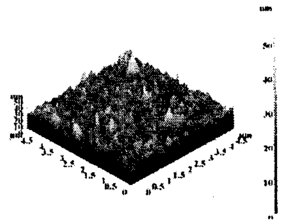
(c)

Fig. 3 FESEM images of NiSi for (a) Ni-V (8nm) (b) Ni-V/TiN (8/25nm) (c) Ni-V/Co/TiN (6/2/25nm) (RTP: 600℃, 30sec, Annealing: 650℃, 30min).

Fig. 4. shows surface roughness that was studied by AFM for all silicides formed with Ni-V, Ni-V/TiN and Ni-V/Co/TiN. Silicide formed with Ni-V (RMS=1.6nm) shows better surface roughness than silicide formed with Ni-V/TiN (RMS=1.7nm) and Ni-V/Co/TiN (RMS=3.5nm) after annealing at 650℃ for 30min.



(a) Roughness=1.6nm **(b) Roughness =1.7nm**



(c) Roughness=3.5nm

Fig. 4 AFM surface roughness of (a) Ni-V (8nm) (b) Ni-V/TiN (8/25nm) (c) Ni-V/Co/TiN (6/2/25nm) (RTP: 600℃, 30sec, Annealing: 650℃, 30min).

4. Conclusion

The nickel silicide properties using Ni-V alloy were studied in this paper. Better thermal stability was achieved by the proposed structure Ni-V compare with Ni-V/TiN and Ni-V/Co/TiN multi-layer structures. Moreover, in case of Ni-V system, more stable sheet resistance was formed with the thicker Ni-V structure.

Acknowledgments

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References

[1] H. Iwai, T. Ohguro, and S. I. Ohmi, Microelectron. Eng., vol. 60, p. 157 168, 2000.

[2] A. Lauwers, A. Streegen, R. Lindsay, A. Satta, H. Bender, and K. Maex, J. Vac. Sci. Technol. B 19 2026, 2001.

[3] C. J. Choi, S. A. Song, Y. W. Ok, and T. Y. Seong, 18th Electronics Letters, vol. 40, no. 6, Mar. 2004

[4] M. C. Sun, M. J. Kim, J. H. Ku, K. J. Roh, C. S. Kim, S. P. Youn, S. W. Jung, S. Choi, N. I. Lee, H. K. Kang, and K. P. Suh, Symp. VLSI Tech. Dig., p.81, 2003

[5] C. Detavernier, X. P. Qu, and L. Van Meirhaeghe, J. Master. Res. 18 1675, 2003.