

Effect of Vacuum Annealing on Thin Film Nickel Silicide for Nano Scale CMOSFETs

Ying-Ying Zhang, Soon-Young Oh, Yong-Jin Kim, Won-Jae Lee, Zhun Zhong, Soon-Yen Jung, Shi-Guang Li, Yeong-Cheol Kim*, Jin-Suk Wang and Hi-Deok Lee
Chungnam National University, * Korea University of Technology and Education

Abstract : In this study, the Ni/Co/TiN (6/2/25 nm) structure was deposited for thermal stability estimation. Vacuum (30 mTorr) annealing was carried out to compare with furnace annealing in nitrogen ambient. The proposed Ni/Co/TiN structure exhibited low temperature silicidation and wide range of rapid thermal process (RTP) windows. The sheet resistance was too high to measure after furnace annealing at 600 °C due to the thin thickness (15 nm) of the nickel silicide. However, the sheet resistance maintained stable characteristics up to 600 °C for 30 min after vacuum annealing. Therefore, the low resistance of thin film nickel silicide was obtained by vacuum annealing at 600 °C.

Key words : Ni silicide, thermal stability, nano scale CMOSFETs

1. Introduction

The self-aligned-silicide (SALICIDE) technology has become an essential part of the fabrication process for recent ultra-high-speed complementary metal oxide semiconductor (CMOS) in ultra large-scale integrated (ULSI) circuits. Recently, nickel mono-silicide (NiSi) has been considered as a viable candidate for contact material because of its low resistivity, relatively low formation temperature, less Si consumption than CoSi₂, no resistivity degradation on narrow lines or gates, and a low Schottky barrier height for holes [1-2]. However, the low thermal stability of the nickel silicide is a major problem for the implementation of NiSi [3-4]. To solve this problem, the uniform layer of NiSi has to be formed on source/drain areas and the silicide film has to withstand the additional thermal budget during back-end processing. It is crucial to prevent both the agglomeration of mono-silicide and its transformation into NiSi₂.

In this study, the Ni/Co/TiN (6/2/25 nm) structure was deposited for thermal stability estimation. Vacuum (30 mTorr) annealing was carried out to compare with furnace annealing in nitrogen ambient. The low resistance of thin film nickel silicide was obtained by vacuum annealing at 600 °C.

2. Experimental

For the experiments, Ni/Co/TiN (6/2/25 nm) layers were sequentially deposited on the p-type Si wafer using RF (Radio Frequency) magnetron sputtering system with Ar ambient. For the Ni silicidation process, the rapid thermal process was carried out at different temperatures in the range of 400-700 °C for 30 s in a N₂ ambient. Unreacted metals and the capping layers were removed by using a

mixture of H₂SO₄ and H₂O₂ with the ratio of 4:1. To test the thermal stability of silicides, samples were furnace annealed in a N₂ ambient and vacuum at three different temperatures for 30 min, respectively.

Sheet resistance was measured using conventional FPP (Four Point Probe). The interface uniformity of the silicide was observed by FESEM (Field Emission Scanning Electron Microscopy, Jeon-Ju branch of the Korea Basic Science Institute, model: Hitach S-4700). AFM (Atomic Force Microscope) and XRD (X-Ray Diffraction) analysis were performed to investigate surface roughness and silicide phase of the silicides, respectively.

3. Results and discussions

Nickel silicides were formed using Ni/Co/TiN tri-layer structure with the thickness of 6/2/25 nm respectively. Fig. 1 shows the sheet resistance of nickel silicide as a function of the formation temperature. It is found that the nickel silicide with Ni/Co/TiN has a wide RTP temperature window until 650 °C.

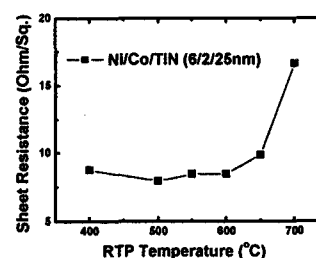


Fig.1 sheet resistance window of nickel silicide with Ni/Co/TiN after RTP.

Fig.2 shows the thermal stability characteristics with different annealing temperature for 30 min. It can be seen

that the sheet resistance is too high to measure after furnace annealing at 600 °C, whereas the sheet resistance after vacuum annealing maintains stable characteristic up to 600 °C.

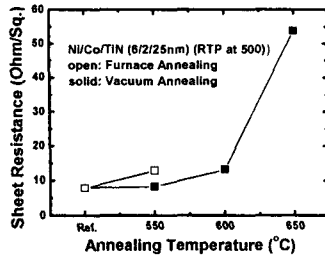


Fig.2 sheet resistance window of nickel silicide with Ni/Co/TiN after annealing.

XRD was used to identify the silicide phase as shown in Fig. 3. Almost same profiles were obtained before and after annealing. But NiSi₂ peaks were observed after furnace annealing 600 °C and vacuum annealing 650 °C.

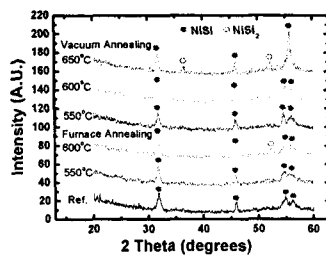


Fig.3 XRD pattern before and after annealing (for RTP at 500 °C).

The cross-sectional FESEM image of nickel silicide before annealing is shown in Fig 4 (a). The good nickel silicide/silicon interface can be seen and about 15 nm thickness can be measured. Figs. 4 (b) and (c) show the images of nickel silicide after furnace annealing in a N₂ ambient and vacuum annealing at 600 °C, respectively.

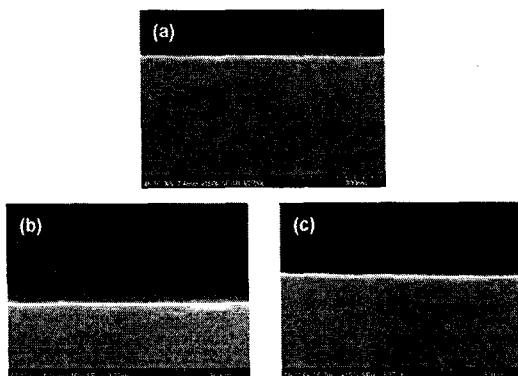


Fig.4 FESEM images of nickel silicide with Ni/Co/TiN (RTP at 500 °C) (a) before annealing, (b) after furnace annealing, and (c) after vacuum annealing at 600 °C.

Clearly, a better interface profile can be observed after vacuum annealing than after furnace annealing in a N₂ ambient. It can explain the very high sheet resistance after furnace annealing at 600 °C.

Fig. 5 shows AFM surface roughness after furnace annealing in a N₂ ambient and vacuum annealing at 600 °C. After vacuum annealing, nickel silicide (Roughness =1.4 nm) shows better surface roughness than that after furnace annealing in a N₂ ambient (Roughness =2.6nm).

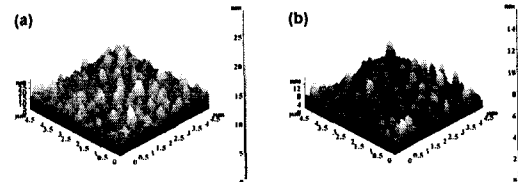


Fig.5 AFM surface roughness of nickel silicide with Ni/Co/TiN (RTP at 500 °C) (a) after furnace annealing, (b) after vacuum annealing at 600 °C.

4. Conclusions

The thermal stability of thin film nickel silicide with Ni/Co/TiN (6/2/25 nm) structure is studied using vacuum annealing compare to furnace annealing. The nickel silicide with 15 nm thickness is obtained. The sheet resistance is too high to measure after furnace annealing at 600 °C. However, the sheet resistance maintains stable characteristics up to 600 °C for 30 min after vacuum annealing. Therefore, the low resistance of thin film nickel silicide is obtained by vacuum annealing at 600 °C.

Acknowledgment

We thank the National Program for Tera-level Nanodevices of the Ministry of Science and Technology as one of the 21 century Frontier Program, and Ying-Ying Zhang thanks Ilun Science and Technology Foundation for support of this work.

References

- [1] T. Morimoto, T. Ohguro, H. S. Momose, T. Inuma, I. kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata and H. Iwai, IEEE Trans. Electron Dev. Vol. 42, No. 5, p.915, 1995.
- [2] A. Lauwers, A. Steegen, M. D. Potter, R. Lindsay, A. Satta, H. Bender and K. Maex, J. Vac. Sci. Technol. B Vol. 19, No. 6, p.2026, 2001.
- [3] F. Deng, R. A. Johnson, P. M. Asbeck, S. S. Lay, J.Appl.Phys. Vol. 81, No.12, p. 8047, 1997.
- [4] M. Tinani, A. Mueller, Y. Gao, E. A. Irene, Y. Z. Hu and S. P. Tay, J. Vac. Sci. Technol. B Vol. 19, No.2, p.376, 2001.