Au 나노입자를 이용한 floating gate memory에서 SiO_2 or SiON 터널링 게이트 산화막의 영향

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Effects of SiO_2 or SiON tunneling gate oxide on Au nano-particles floating gate memory

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Abstract : Floating gate non-volatile memory devices with Au nano-particles embedded in SiON or SiO_2 dielectrics were fabricated by digital sputtering method. The size and the density of Au are 4nm and 2×10^{12} cm^{-2}, respectively. The floating gate memory of MOSFET with 5nm tunnel oxide and 45nm control oxide have been fabticated. This devices revealed a memory effect which due to programming and erasing works perform by a gate bias stress repeatedly.

Key Words : Floating gated non-volatile memory, nano-particles, Au/SiON/SiO_2

1. Introduction

Demand for high density and high performance non-volatile memory has rapidly grown portable electronic devices, such as cellular phones and digital cameras. Although the scaling down of devices is essential for the high-performance flash memory, a conventional flash memory technology has various problems. The thickness of the tunneling gate oxide in a conventional flash memory device can not be scaled down with the device size due to the difficulties of keeping the excellent charge retention and endurance characteristics. In order to overcome the limits of scaling down in the flash memory technology, new non-volatile memories such as Si quantum dot memory and SONOS (silicon-oxide-nitride -oxide-silicon) memory have been proposed. However, the density of charge retention sites and the uniformity of memory window are not sufficient in these memories [1-3].

In this work, we propose floating gate non-volatile memory devices with Au nano-particles embedded in SiON or SiO_2 dielectrics using digital sputtering method and compare with the electrical characteristics.

2. Experiments

MOS capacitors with Au film of 1 nm thickness in dielectric of different composition such as SiO_xN_y were fabricated to optimize the metal nano-particle formation process conditions. The floating gate memory of MOSFET with Au nano-particles were fabricated on the p-type *UNIBOND SOI* wafers with a 100 nm top Si layer and a 200 nm buried oxide layer. The thickness of tunneling oxide(SiO_2 or SiON) was 5 nm by using sputtering method. After the deposition of 1 nm thick Au thin film as metal nano-particles, the deposition of control oxide(SiO_2 or SiON) with 45 nm was followed by sequential sputtering. The Au nano-particles were annealed at 800 ℃ for 10 s to remove the surface defects because the surface defects play a role of charging sites between insulator and Au nano-particles. The aluminum layer with a 200 nm was deposited on the control oxide and the patterning of gate electrode was followed. Finally, the phosphorus plasma doping at elevated temperature was carried out for source-drain doping [4]. The NFGM (nano-floating gate memory) devices were analyzed by measuring the programing/erasing characteristics.

3. Results and Discussion

Figure 1 shows C-V curves of the MOS capacitors which contains 1 nm Au film in dielectric of different composition such as SiO_xN_y. The C-V curve of $SiO_{1.3}N_1$ appeared regular form [5].

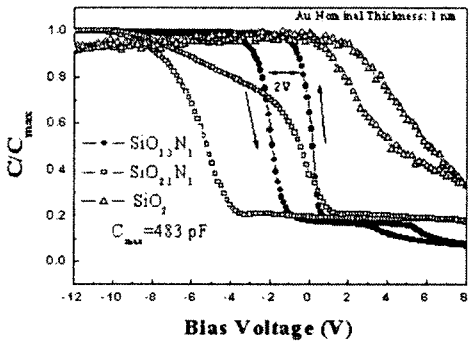

Figure 1. C-V characteristics of MOS capacitors

Figure 2 shows that TEM images of Au particles using 1 nm thickness Au film. The average diameter of particles was 4 nm and the density was 2×10 cm^{-2}. The shape of particles in $SiO_{1.3}N_1$ is clearer than that of particles in SiO_2 matrix.

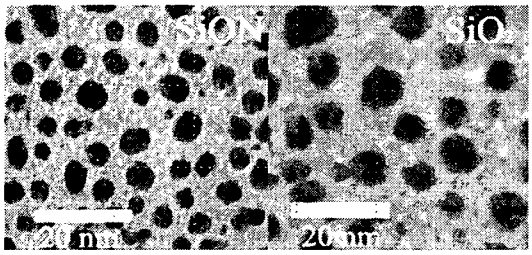

Figure 2. TEM images of the Au nano-particles formed by Au film with the nominal thickness 1 nm.

Figure 3 shows the memory window and the retention characteristics of Au nano-particles NFGM. The memory window due to the threshold voltage shift was about 2 V and 1.5 V in the $SiO_{1.3}N_1$ or SiO_2 matrix, respectively. However, the memory window was decreased rapidly as time elapse. The reason of this degradation is considered to be a leakage current through $SiO_{1.3}N_1$ or SiO_2 tunneling barrier because there are many defects.

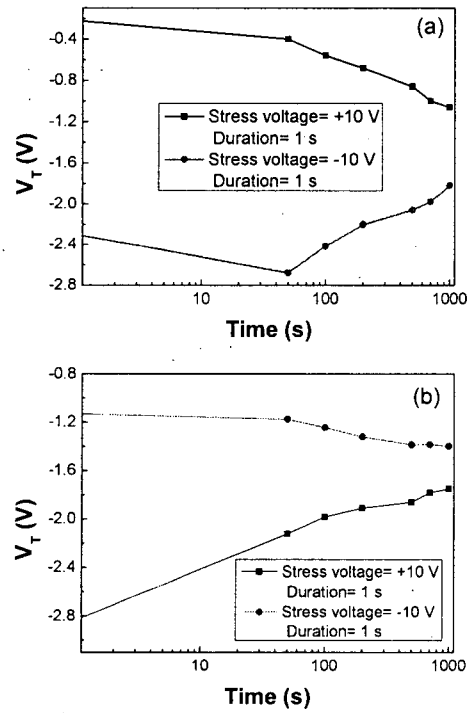

Figure 3. Retention time of NFGM with Au nano-particles embedded in (a) $SiO_{1.3}N_1$ and (b) SiO_2 dielectrics

4. Conclusions

In this study, the NFGM devices were fabricated with Au nano-particles embedded in $SiO_{1.3}N_1$ or SiO_2 dielectrics by digital sputtering method. The memory window due to the threshold voltage shift was about 2 V and 1.5 V in the $SiO_{1.3}N_1$ or SiO_2 matrix, respectively. It is found that the V_{th} window was maintained about 0.8 V and 0.6 V after an electrical stress of 10^4 s in the $SiO_{1.3}N_1$ or SiO_2 matrix, respectively. The $SiO_{1.3}N_1$ matrix showed better electrical charging properties than the SiO_2 matrix. We expect that the metal nano-particles are advantageous to apply highly integrated non-volatile memory device by improving the quality of $SiO_{1.3}N_1$ matrix.

5. References

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