Extreme baking effect of interlayer on PLED's performance

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Abstract

Through baking process on an interlayer, known as hole transporting layer, varying baking temperature up to 300 degree, which is considered as extremely high for polymer light emitting device (PLED) system, we found interesting relationship between packing density and morphology affecting device performance. Granular morphology shows that as temperature increases, grain size is getting smaller to pack closely and make interlayer harden. Such denser interlayer has temperature dependency of its own mobility, even without clear evidence of degradation of material itself. Its fact proven in a single film also reflects on multilayered PLED's performance like IVL, efficiency, lifetime. It's found that, especially, to enhance lifetime is related with thermal stability of interlayer and its mobility dependency to meet better charge balance. Therefore, it gives us understanding not only baking effect of interlayer, but also material & device designing guide to enhance lifetime.

1. Introduction

Among organic light emitting materials, polymer has its stand on OLED application as a prospective cost-down factor for mass production in future. Recently, there's promising reports on performance of polymer light emitting device (PLED). Its developing pace looks like chasing the performance of small molecule at a rapider rate ever since 1990's. But still, there's historically always a gap between high and low weighting materials. Should these high and low weighting materials make their ability keep apart as along with their verbal meanings? Most of people working on OLED and its application field, I think, believe that such fact could be overcome soon or later and encourage us to research and develop. Even more, one issue, i.e., "market is impatient" accelerates and pushes us into deep ocean, over which "blue ocean" locates hopefully.

We've already reported failure mode analysis of blue PLED in IMID/IDMC last year.[1] Insoluble layer started to form on the side of anode where emitting zone located. The growing insoluble layer from PEDOT side into emitting layer was fatal to device performance, especially, lifetime. It's known that insertion of interlayer between PEDOT and emitting layer could enhance lifetime by at least few times to more than ten times depending on kinds of polymer.[2] Such improvement was shown in our previous study as well. But, detail physical mechanism of interlayer is unclear up to now.

One of interesting point is how it works within multilayered system, in which interlayer is not, frankly speaking, well-defined layer due to its solubility issue, i.e., when using solvents with similar solubility power like toluene and xylene for emitting layer and interlayer, respectively. But, we already had a lot of experience to make multilayered polymer system, while partially sacrificing top surface of interlayer as we spin another polymer layer on top of that. Thus, in this study, we focus on the working mechanism not by simply varying baking temperature within generally accepted 200~220 degree, but by baking extremely up to 300degree. Then, we observed mechanical and electrical behavior of single interlayer film and interlayer-inserted PLED to see what happens inside.

2. Results

We made two sets of PLED. One is ITO/PEDOT 50nm/ SI5 (SAIT's interlayer)40nm/$BaF_2$5nm/ Ca3nm/Al150nm, making interlayer as emitting layer. The other is ITO/PEDOT50nm/SAIT5 40nm/SB9 (SAIT's blue polymer) 60nm/$BaF_2$5nm/Ca3nm/Al 150nm. Each set has been baked to a maximum temperature of 300degree.

We have to confirm two things to do. One is to know how PEDOT survives when baking interlayer at an extremely high temperature. We try to apply the

almost same thermal power when baking interlayer above PEDOT to make PLED. Thus, at 300degree, we baked for maximum 10mins making the two sets of devices. To know any material degradation is the other thing, which was carried out through measuring photo-luminescence for each film. We found no obvious variation of spectral shape within visible range.

Recently, we measured the packing density of neat film using AFM and obtained relationship with device lifetime, which is under preparing for a paper. In that study, we found such physical packing density as one of critical factors to analyze and/or predict device performance. That makes us to apply such method to investigation of single interlayer films depending on baking temperature.

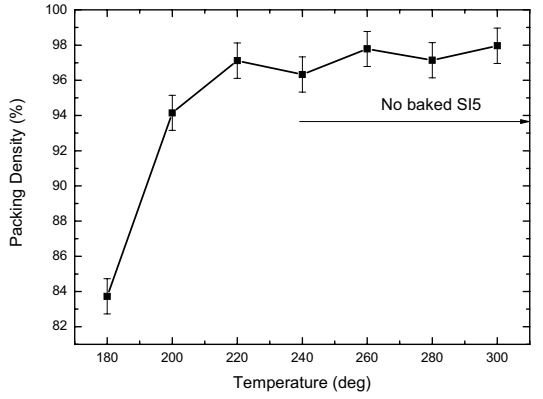

Figure1. Packing density depending on baking temperature of SI5 (square) and PFB (circle). An arrow represents packing density of SI5 without baking.

Single interlayer film with a thickness of 40nm was spin-coated and baked at different temperature. Fig.1 plotted temperature dependency of packing density of SI5 (SAIT's new interlayer) comparing to SI5 film without baking. As the temperature increases from 180 to 300 degree, packing density also increases fast at around 200degree and, then, slowly at higher than 220degree. Since glass transition temperature (Tg) of SI5 was about 250degree, we simply expected that packing density would have a maximum at around the Tg. Considering slow increase of packing density over 220degree, we guess that such behavior of packing density could come from the difference of Tg between thin film and bulk, and could be related with surface morphology.

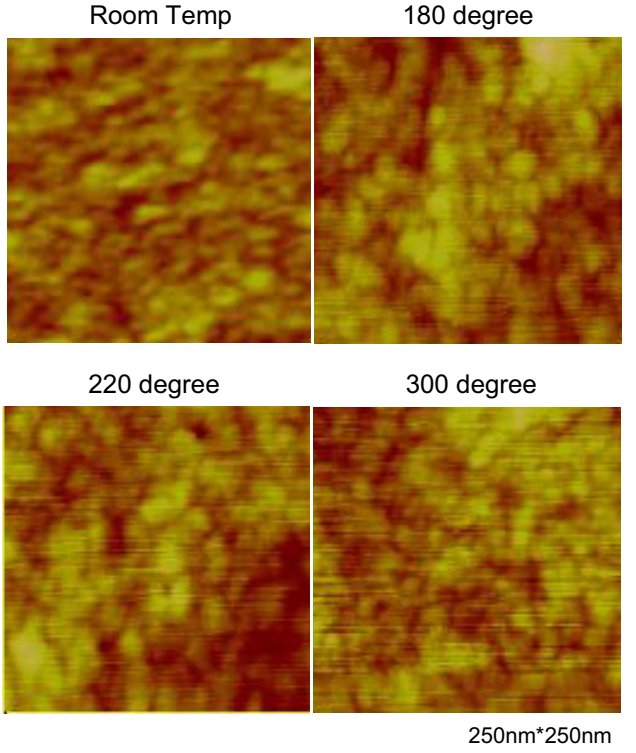

Figure2. AFM results on differently baked SI5 single film.

Fig2. shows surface morphology of SI5 films using AFM . Basically, after baking process, all films have granular morphology. When we increase baking temperature, grain size is reduced. With relating to results of packing density in Fig.1, it could be expected that these smaller grains makes the film harden reducing free volume between them.

With knowing physical behavior of SI5, we tried to investigate its electrical properties measuring transient electroluminescence (TEL) for above two sets of devices in Fig.3. There are two things to notify. For all two sets of devices, the trend of temperature dependency is similar. It means that solubility issue between interlayer and emitting layer is not effective. According to increasing baking temperature of interlayer, reducing initial slope of luminance indicates lower mobility of carrier.

From independent experiments, we found that emitting SB9 layer has higher electron mobility and

SI5 interlayer higher hole one. Then, such mobility behavior comes from variation of hole mobility. It could be inferred from above morphological behavior that lower grain size generates larger number of grain boundary, which requires higher energy to go through and eventually makes its mobility low. Additionally,

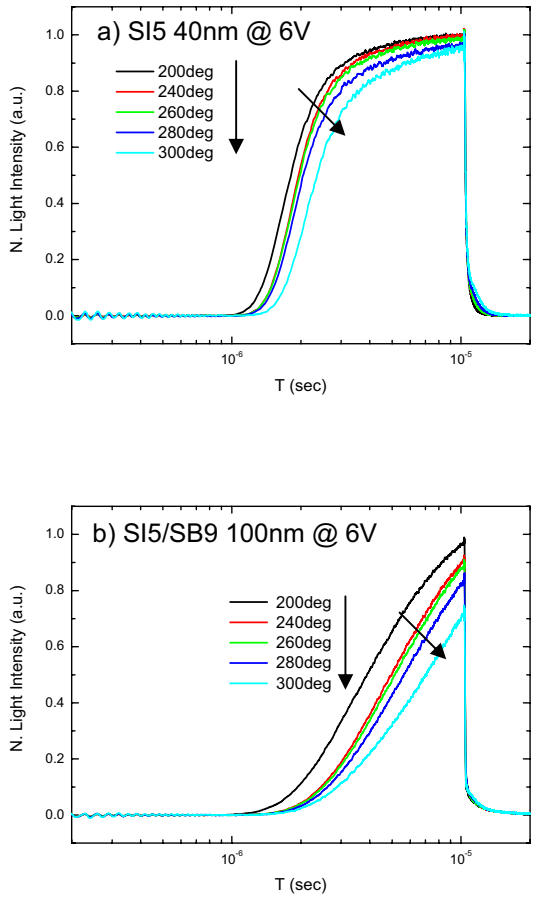

Figure3. Transient EL results on two sets of devices with pulse duration of 10μsec and 6V. Arrows indicate increase of temperature and its corresponding change of TEL signal.

larger number of grain boundary is easy to generate trap sites. In Fig3. there are concrete evidence of trap sites by notifying turn-off part of TEL signal.

Such variation of hole mobility of interlayer naturally affects device performance, specifically, charge balance within recombination zone. Current efficiency in Fig.4 explains well and shows almost 17% difference depending on variation of hole mobility.

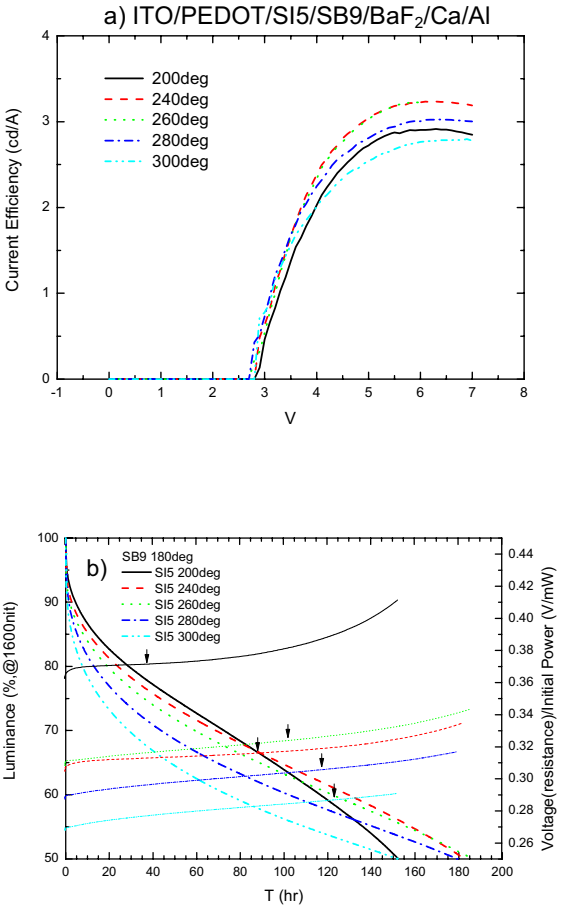

Figure4. a) Current efficiency of devices. b) Life curves with its varying voltage (resistance in constant current mode) depending on baking temperature of interlayer. Black arrows indicate a point where voltage changes slope. SB9 has been baked at 180 degree.

More importantly, lifetime has a maximum at around Tg of SI5 interlayer, where device shows better charge balance via changing hole mobility influenced from physical surface morphology depending on baking temperature. Thus, it is important to note that, for better device performance, we should consider granular interaction affecting carrier balance even just in polymer system. If we extend the meaning to small molecular system intermolecular interaction could draw strong attention for better output, which will our next concern of research.

Interestingly, 200 and 300 degree life curves have different shapes but the same lifetimes with similar

current efficiencies. From above results, it could be understood in relationship between physical packing density and hole mobility. As indicated by black arrows in Fig.2, points of voltage slope change, I think, could be in relation with packing density representing thermal stability of interlayer. Thus, for polymer system having recombination zone located at the anode side, it is important to control stable injection and transport of hole during operation.

3. Conclusion

We investigated extreme baking effect of interlayer by measuring physical packing density, surface morphology, transient EL to understand relations with device performance. In the polymer system, granular structure was naturally generated. Smaller grain size via increasing baking temperature make hole mobility of interlayer low while increasing physical packing density. It is important to make balance between physical hardness and carrier mobility, which technology would be a way to control a life curve and such understanding could help researchers develop better material and device for upcoming OLED generation, I hope.

4. Acknowledgements

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5. References

[1] M.G.Kim, et. al., IMID'05 P154.

[2] J.S.Kim, et. al., APL **87**, 023506 (2005).