Uniformity Optimization of TFTs Fabricated on 2-shot SLS-Processed Si Films

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Abstract
Nonoptimal placement of short-channel-length TFTs in large-grained polycrystalline Si films with a periodic microstructure, as for instance obtained via 2-shot SLS, can potentially lead to degradation in the overall uniformity of the resultant devices. In this paper, we explain and demonstrate that by simply introducing a well-defined misorientation between the devices and the periodic microstructure, it is possible to significantly reduce (and potentially entirely eliminate) the device nonuniformity problem that can arise from such a cause.

1. Introduction
Sequential lateral solidification (SLS) is a flexible crystallization method that has been demonstrated to be capable of creating a variety of low-defect-density polycrystalline Si films on glass and plastic substrates [1,2]. In general, SLS can be characterized as an iterative-type pulsed-laser-based process that at least involves the following technical steps: (1) localized complete melting of predetermined area(s) of the film leading to controlled super-lateral growth [3] and (2) relative repositioning of the sample with respect to the beam such that the large-grained material grown via lateral solidification during the prior pulse will seed epitaxial lateral growth during the following irradiation.

Currently, SLS-processed Si films with a particular microstructure, which is referred to as the "2 shot" SLS microstructure, are being successfully employed for manufacture of advanced AMLCDs [4]. It should be noted that this 2-shot microstructure corresponds to one of many low-defect-density microstructures that can be generated using SLS [3]. (Other salient examples include the directionally solidified microstructure and location-controlled single-crystal regions.)

The microstructure of a 2-shot material can be described as essentially consisting of rows of elongated grains that are periodically arranged (Figure 1). As a result, one salient and intrinsic microstructural feature of the material pertains to the existence of regularly spaced high-angle grain boundaries that run perpendicular to the elongated direction of the grains. The apparent anisotropic character of the microstructure has been found to exert a definite influence on the resultant devices; optimally performing devices have been obtained when the source-to-drain direction of the devices is made approximately parallel to the elongated direction of the grains [5]. As such, it has become customary to adopt this device orientation for fabricating high-performance TFTs on the material.

In any case, 2-shot microstructured Si films are noteworthy because they can be efficiently produced either using a 2-dimensional projection-type SLS system by utilizing the continuous-scan technique [4,6] or, alternatively, via the line-scan SLS approach [7] by (1) preventing any nucleation from taking place within the irradiated area and (2) by translating the sample, in the direction parallel to the elongated direction of the grains, more than — but less than twice — the single-pulse-induced lateral growth distance, between the pulses [5]. These 2-shot SLS

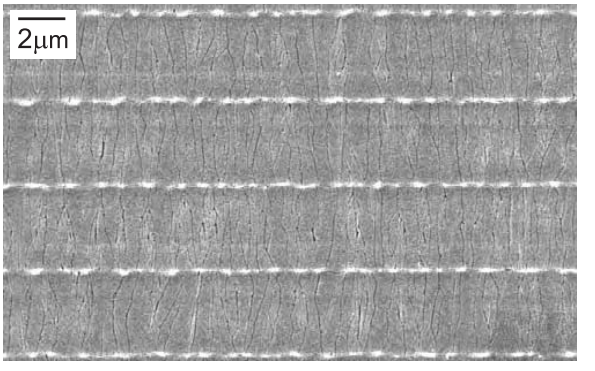

Figure 1: SEM image of a defect-etched 100-nm-thick Si film crystallized via a 2-shot SLS process. This particular SLS microstructure is (1) referred to as the "2 shot" microstructure, (2) can be generated using several SLS schemes, including line-scan SLS, and (3) corresponds to just one of many low-defect-density microstructures that can be generated via SLS.

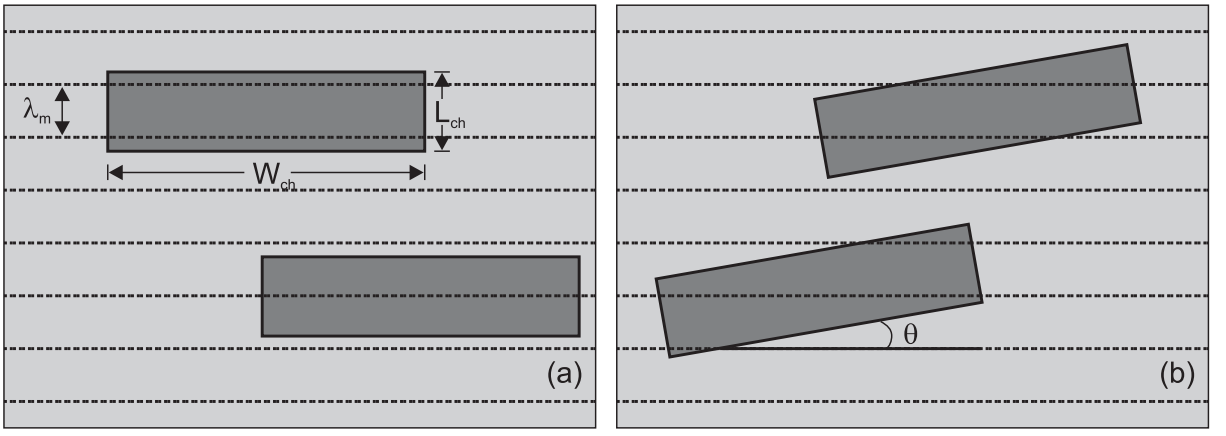

Figure 2: Schematic diagrams that are drawn to illustrate the concept behind the tilt-engineering method. Shown are TFTs that have been "randomly" placed within a periodic microstructure with (a) no relative tilting whatsoever, and (b) an optimal tilting between the device active area and the microstructure periodicity (with m = 1 in Equation (1)). In the figure, W_{ch} and L_{ch} are the device channel width and length, respectively, λ_m is the microstructure periodicity, and θ is the tilt angle.

processes are particularly significant, as far as manufacturing is concerned, because they can be configured to achieve extremely high effective crystallization rates (i.e., ~ 50 to 100 cm^2/sec for Gen 4 substrates using presently configurable SLS manufacturing systems [8,9]).

The overall quality of 2-shot materials may justly be viewed as occupying the lower end of the microstructure-quality spectrum that can be generated by SLS. Nevertheless, the 2-shot material may still possess the right combination of microstructural attributes to potentially establish itself as the material of choice, as far as the active-matrix display manufacturing is concerned. The material, for instance, (1) is recognized as being superior to the other materials that are produced using alternative manufacturing-compatible crystallization techniques, (2) has proven itself to be entirely compatible with actual manufacturing of AMLCD products, and (3) is in the process of increasingly and rapidly becoming capable of addressing the future device-related needs associated with SOG AMLCDs and large-sized AMOLED displays. Such combination of strategically and tactically important factors (i.e., sufficiently good materials being produced with the most desired manufacturing and processing attributes) is what could potentially make the 2-shot SLS method, as far as the LTPS flat-panel-display industry is concerned, the most compelling manufacturing choice.

2. Device Placement in 2-Shot SLS Materials

In general, it is possible to envision two distinct scenarios for placing TFTs in 2-shot SLS materials. Ideally, one would explicitly control the relative placement of the devices with respect to the locations of the perpendicular grain boundaries so that all TFTs could result in having an identical active-channel microstructure.

Technically, however, it is substantially easier to exercise an essentially trivial alternative option in which devices are randomly placed on the material without giving any consideration whatsoever regarding their placement with respect to the microstructure. When this approach is implemented, a device uniformity issue may potentially be encountered due to the variations in the exact amount and relative locations of the perpendicular high-angle grain boundaries within the active channel area, even for a set of identically shaped devices (Figure 2).

Such an effect could be negligible when the channel length is much greater than the 2-shot grain length. Conversely, the effect should become increasingly noticeable as the channel length is reduced and could become rather significant as it becomes comparable to the grain length. Given that the overall uniformity of TFTs is increasingly being viewed as one of the more important performance characteristics of the devices (for both SOG AMLCDs and AMOLED displays), and further that increasingly smaller devices with shorter channels are being fabricated, one could ill afford to overlook such an issue.

In this paper, we present experimental results that lend support to a geometrical solution, referred to as "tilt engineering", which we have previously proposed to address the above-stated problem that can

arise in low-defect-density materials with a periodic microstructure.

3. Device Tilt Engineering

The tilt engineering solution builds on recognizing the geometrical origin of the above problem; therefore, it seeks to remedy the situation by providing a geometrical solution. The tilt-engineering concept recognizes how it should be possible (1) to at least reduce the microstructure-variation effect by introducing some orientational tilting of the microstructure relative to the devices [10], and (2) to identify the optimal tilt angle(s) at which the effect can be geometrically eliminated.

The optimal angle of relative misorientation, $\theta_{optimal}$, at which random placement of devices within a periodically microstructured material will result in the devices having equivalent-microstructured active channel regions, can be determined from purely geometrical considerations as

$$\text{Eq. (1)} \qquad \theta_{optimal} = \arcsin\left(m \frac{\lambda_m}{W_{ch}} \right)$$

where W_{ch} is the width of the active channel region, λ_m is the periodicity of the microstructure (e.g., the spacing between the perpendicular grain boundaries in the case of a 2-shot SLS-processed material), and m is a positive integer less than W_{ch}/λ_m. The most preferred of m is 1, for this number yields the smallest optimal tilt angle; increasing the tilt angle gradually reduces the mobility of the devices, among other things, due to the degrading influence of the previously "parallel" boundaries becoming increasingly significant to the flow of charge carriers.

It is easiest to visualize how the tilt engineering method works by considering, for instance, the "number" of perpendicular grain boundaries that are present within the active channel portion of a device. When TFTs are intentionally tilted with respect to the 2-shot SLS microstructure at one of the optimal tilt angles described above, the exact "amount" of now slightly off-perpendicular grain boundaries within the active channel area of the devices becomes a single-valued quantity that is effectively invariant to any arbitrary translational operation of the devices. (A similar point can be made as regards the effective microstructure that is manifested within the channel region of the devices.) The significance here being that TFTs can now be placed anywhere within the material and not suffer from the periodic-microstructure-induced device nonuniformity. (The scheme is just as applicable in the case where long-and-narrow channel devices with multiple grain boundaries are present in the region, as illustrated in Fig. 4(a))

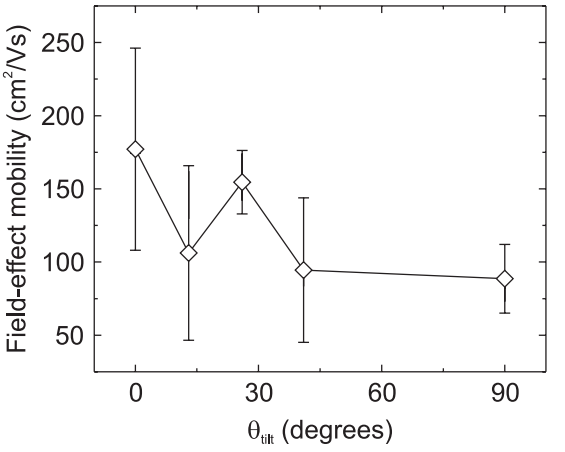

Figure 3: Field-effect electron mobility as a function of the relative tilt angle between the channel and the microstructure. The error bars represent the maximum-minimum scatter measured over 42 TFTs.

4. Experimental Details and Results

The substrates used in this study were 6" quartz wafers. The 100-nm-thick a-Si layer was deposited on the substrates via PECVD, and the samples were dehydrogenated via thermal annealing prior to laser irradiation. The SLS irradiation system utilized in this work consisted of an excimer laser operating at 308nm (XeCl), a laser pulse extender (used to increase the pulse to ~220ns (FWHM)), a 5× demagnification projection system, and a submicrometer-precision translation stage. The mask illuminated by the projection system was fabricated using chrome-on-quartz mask plates.

The continuous-scan SLS scheme was employed to convert the entire Si film into a 2-shot microstructured material with the perpendicular grain boundary spacing of 3.5μm. No position-sensitive-firing scheme or location-control methods were employed (other than controlling the relative misorientation of the devices); in effect, the TFT devices were placed randomly with respect to the locations of perpendicular grain boundaries.

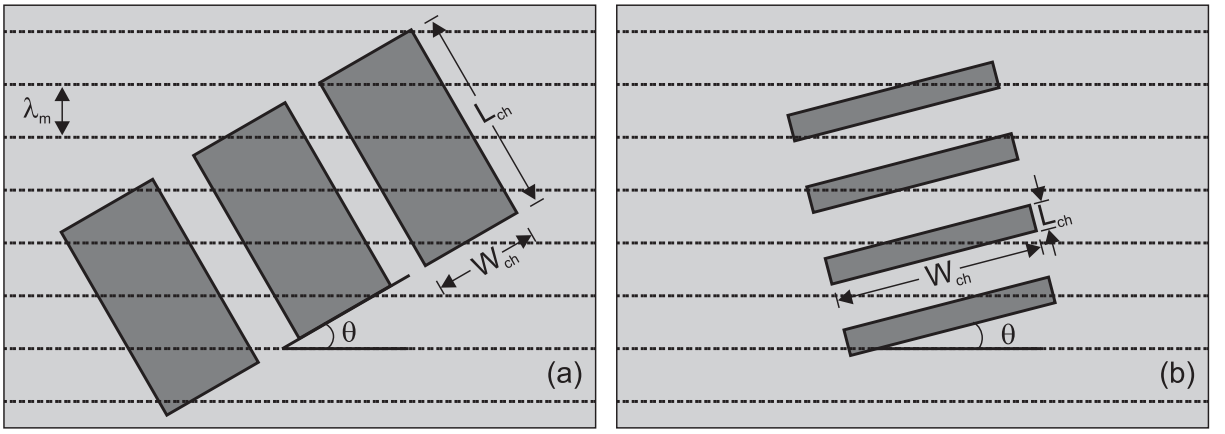

Figure 4: Schematic diagrams showing additional examples of optimally tilt-engineered devices (with m = 1 in Equation (1)) corresponding to (a) long-channel-length/short-channel-width devices and (b) short-channel-length devices where L_{ch} is less than λ_m.

Variation of the tilt angle, θ_{tilt}, between device channel width and perpendicular lying grain boundaries was introduced by carrying out tilted crystallization of the wafers. The misorientation of the wafers were experimentally accomplished by using custom machined shims to position the wafer with the desired tilt angle on the vacuum chuck during the crystallization step. The device channel width was 8μm, and misorientation angles were selected to be 0°, 13°, 26°, 41° and 90°. All samples were crystallized at the same energy density.

After SLS crystallization, the Si films were patterned into active device islands. A 100nm SiO_2 layer was then deposited for the gate dielectric, followed by deposition and subsequent patterning of a poly-Si gate structure. Ion implantation was then simultaneously carried out for the source region, drain region and gate electrode. The phosphorus implant was performed at 40 keV with a dose of $3x10^{15}$ cm^{-2}, and the dopant activation was accomplished via thermal annealing at 650 °C for 5 hours. (Only n-channel TFTs were made in this study). A Ti/TiN/AlCu multilayer stack was sputter deposited and patterned to form metallic contact pads. This was followed by a forming gas anneal for 30 minutes at 350 ºC. Following the metallization steps, the TFTs were subjected to plasma hydrogenation for 15 minutes at 320 ºC.

The analysis of resulting TFTs was carried out using a Hewlett-Packard 4145B semiconductor parameter analyzer connected to a manual probe station. 50 devices were measured over 25 die spanning an area of ~9.8 cm by 7 cm. The 4 lowest and highest performing devices were removed from the data sets, so as to remove their influence on the statistics analysis (some of these devices appear to be malfunctioning devices, as they performed in an abnormal manner). The field-effect mobility for each device was calculated from the maximum measured transconductance with the drain biased at 0.1 Volts. The resulting field-effect mobility data for devices with channel lengths of 2μm are plotted as a function of misorientation angle in Figure 3.

For those TFTs made with channel lengths less than the perpendicular grain-boundary spacing, a bimodal distribution of the field-effect electron mobility was observed (as can be anticipated from simple geometrical considerations). In fact, a direct device performance-microstructure correlation was confirmed to take place between the device's performance and the presence or absence of a perpendicular lying grain-boundary within the active channel region.

The minimum device-to-device scatter for this set of TFTs was observed to take place at the optimum tilt angle (which was 26° for the devices shown in Figure 3). A relative maximum in the field-effect mobility was also found to occur at this angle. Although our devices were fabricated using the processing steps and procedures that admittedly are not fully optimized (and the consequence of which are reflected in rather nonoptimal performance characteristics of the fabricated devices), overall, we conclude that the experimental results we have obtained in this work can be interpreted as unmistakably substantiating (1) the existence of the nonuniformity issue being discussed in this paper and (2) the validity of the tilt-engineering scheme to address the situation.

5. Discussion

The applicability of the tilt-engineering concept is not limited to the 2-shot microstructure, per se. The basic idea of the method can be recognized as being very general, and as such, should be applicable to other materials with periodic microstructural features. Such materials include those that can be generated using other SLS schemes and variations [11-13].

In addition to the well-appreciated effect as regards the number of grain boundaries that are present within the active device area, it is possible to further identify additional microstructural details and factors that can also influence the performance of devices. Here, potentially detrimental influences that can arise from such causes may also be addressed via the tilt-engineering method, provided that they appear in a regular and periodic manner. For instance, it is known that the exact location of grain boundaries close to the drain region of a device can play a critical role in determining the electronic behavior of the device [14]. When all TFTs are tilted with the optimal degree of misorientation, it can be seen that the resulting devices will possess an effectively equivalent spatial allocation of grain boundaries within the active channel area, and can therefore be expected to perform more uniformly.

It is also possible to identify the surface morphology of Si films manifested within the active device area as a factor that may have some influence on the device performance; here, the degree of surface roughness is thought to have an effect on the scattering of charge carriers at the interface. If the crystallized films were to posses a periodic surface undulation (which, for instance, is definitely the case with the 2-shot microstructure, and, to a lesser extent, is also the case with directionally SLS-processed Si films), then tilt-engineering may just as effectively be applied to reduce any influence such periodic surface undulation could have on the device-to-device uniformity.

Finally, we would like to comment on the utility of 2-shot microstructured Si films by pointing out the possibility of obtaining ultra-high mobility TFTs from these films, should such devices be deemed desirable or necessary. Here, it is easy to imagine how the average mobility of 2-shot TFTs can be increased to ultimately approach the level typically associated with the SLS TFTs that are made on directionally solidified Si films — simply by reducing the device channel length of the 2-shot TFTs to become substantially smaller than the length of the elongated grains (Figure 4(b)). Various findings and considerations indicate that such short-channel 2-shot TFTs, when optimally fabricated in accordance with the tilt-engineering method (and possibly employing the hybrid SLS approach [15]), may end up providing the ultra-high mobility TFTs that are more uniform than those that can be realized using the directionally solidified Si films obtained via SLS.

6. Conclusion

When properly implemented, the tilt-engineering method can circumvent the potential nonuniformity problem that can arise when short-channel-length devices are randomly placed on periodically microstructured Si films. The method accomplishes this by virtue of creating an effectively equivalent active-channel microstructure for a given set of devices. Using our ability to control the dimensional details of the microstructure, devices were fabricated having various degrees of misalignment between the active channel area and the microstructure to demonstrate the effectiveness of the tilt-engineering technique.

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