# Development of nanocrystalline silicon thin film transistors with low-leakage and high stability for AMOLED displays

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## Abstract

*Nanocrystalline silicon (nc-Si) based TFTs were developed using a conventional PECVD production system. Devices exhibit very interesting characteristics, in particular when using a bi-layer structure which reduces leakage current and improves subthreshold area. Good stability and low leakage current make these devices suitable for the fabrication of low-cost and high performance AM-OLED displays.*

## 1. Introduction:

Amorphous silicon (a-Si) thin film transistors (TFTs) are extensively used as switching element for active-matrix liquid crystal displays. However, one of the most serious problems of such devices is the low reliability evidenced by important shift of the threshold voltage, which makes these devices not suitable for active matrix OLED displays, where a high stability is required for the driving TFT. For many years, nanocrystalline silicon has been evidenced as a good alternative to a-Si, providing much more stable devices, and slightly higher mobility [1,2]. However, in general, little attention is paid to the leakage current, which should remain as low as possible, in particular for the switch transistor of the OLED pixel. In this paper we present the development of high stability and low-leakage nc-Si TFTs, and their potential use in high performance and low-cost AMOLED displays.

## 2. Experimental:

Thin film transistors were made using the conventional bottom gate, back channel etched structure, as shown on Figure 1. More details on the process can also be found elsewhere [3].

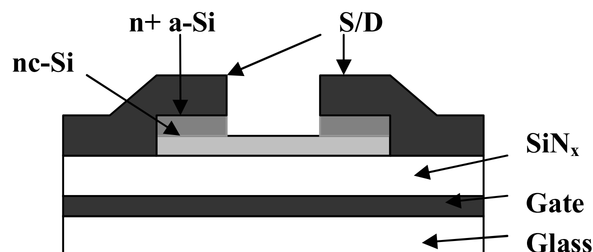


**Figure 1. Cross section of BG-BCE TFTs**

Nanocrystalline silicon films were grown on top of silicon nitride ($SiN_x$) under layer by standard 13.56 MHz radio-frequency glow-discharge technique using $SiF_4$, Ar, and $H_2$ gas feedstock. All layers, constituents of the TFT, were deposited sequentially in a conventional Capacitively Coupled Plasma tool (Unaxis PECVD Kai XL). After growth of nc-Si film, a thin n+ doped amorphous silicon (n+ a-Si) layer is deposited. Also, devices with an additional layer of a-Si between nc-Si and n+ a-Si (so-called: “bi-layer”) were fabricated for comparison with former ones (“monolayer”). Then a thick Mo layer was deposited and patterned for source and drain contacts. Source and drain electrodes were then used as a mask to etch the n+ a-Si (back-channel etch process). The operation was monitored by using a laser for a finely-controlled etching. Then active regions were patterned

by plasma using an Inductively Coupled Plasma tool (Nextral ICP 860 IL) with $Cl_2$ as reacting gas. After $SiN_x$ passivation deposition, the source, drain, and gate contacts were opened through the passivation and gate insulator layers. Prior to electrical characterization, one hour annealing at 200 °C has been performed. After annealing, transfer $I_{DS}$-$V_G$ and output $I_{DS}$-$V_{DS}$ characteristics have been measured using an Agilent 4156B device parameter analyzer.

## 3. Results and discussion:

Structural properties of the nc-Si layers: We analysed nc-Si layers having a thickness of 170 nm. The surface of the nc-Si was characterized by AFM, as it can be seen on Figure 2. The surface roughness is in the order of 4 nm. The structural properties of the nc-Si films were investigated by transmission electron microscopy (TEM) analysis. Plane-view TEM micrographs (Figure 3) have shown that the grains exhibit a mean size of about 45 nm, with the maximum and minimum grain size being 80 nm and 8 nm, respectively.

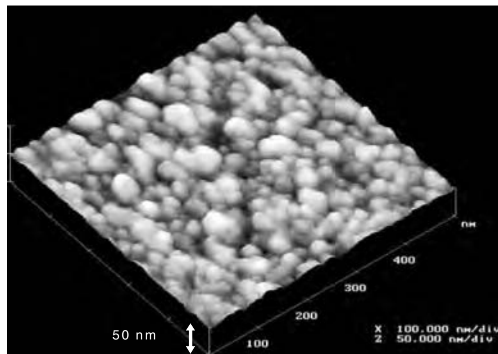


**Figure 2. AFM analysis of nc-Si surface.**

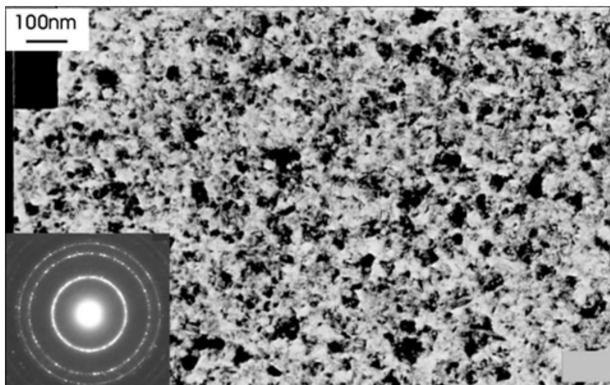


**Figure 3. TEM plane-view of nc-Si layer. The inset shows diffraction pattern.**

The diffraction pattern confirmed the nanocrystalline nature of the grains, whereas no preferential growth of the grains was found.

Electrical characterization: After TFT fabrication, electrical characterization was carried out on the devices. Figure 4 shows the transfer characteristic of a typical nc-Si TFT with the monolayer structure. It is important to notice that device was measured at $V_{ds}$ = 10 V; which corresponds to conditions where high field in the drain region drastically enhances leakage current.

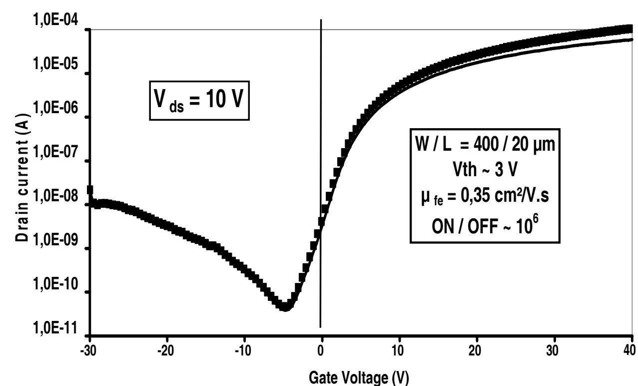


**Figure 4. Transfer characteristic of nc-Si TFT with dimensions of W = 400 µm and L = 20 µm.**

The threshold voltage ($V_{th}$) and mobility (µ) values are 3 V and 0.35 cm²/V.s, respectively. As it can be seen, the leakage current is about 2. $10^{-11}$ A at $V_g$ = -5 V, which is quite low when considering the high $V_{ds}$.

Leakage current at high negative Vg: However, at higher negative $V_g$ (i. e. less than -20 V), leakage current increases significantly, which is penalizing even if TFTs are not polarized at such voltages under normal display addressing conditions. This strong increasing of leakage current under high field in the drain area have been already observed in nc-Si TFTs [4], and looks similar to the case of poly-Silicon TFTs, for which the leakage current under this regime has been evidenced as the result of band-to band tunneling [5].

Current in the subthreshold area: When focusing to the area of $V_g$ around zero Volt, one observe a quite degraded subthreshold area, with a slope of 1.8 V/dec. In the mean time the device is not fully blocked at zero Volt. The behavior in the low negative

subthreshold region has been already identified as reflecting back-channel conduction [6]. Moreover, we recently showed that undesired back-channel conduction is observed on nc-Si TFTs, and evidenced that it is the result of backchannel contamination by oxygen [3]. This tends to indicate that nc-Si is more sensitive to contamination than a-Si.

An output characteristic is shown on Figure 5; the curves indicate good source/drain contact, and no crowding contact effect.

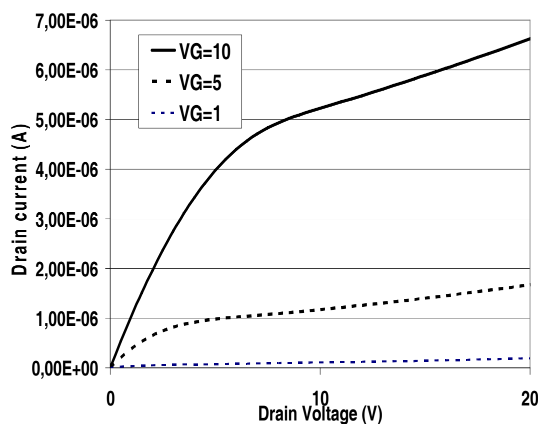


**Figure 5. Output characteristic of nc-Si TFT with dimensions of W = 400 µm and L = 20 µm.**

Bi-layer devices:

Figure 6 shows transfer characteristic of a nc-Si device with the bi-layer structure.

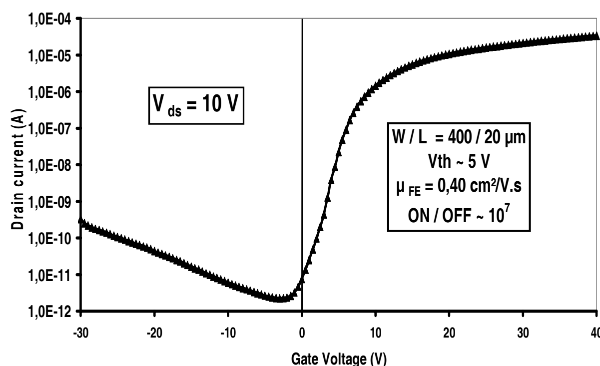


**Figure 6. Transfer characteristic of nc-Si TFT with bi-layer structure.**

The device performance is strongly improved. In particular, the leakage current is drastically reduced, both at low and high negative gate voltage. In the mean time, the subthreshold region is greatly improved, with a slope of 1.1 V/dec. Also, the device is actually blocked for a gate voltage of zero. The presence of the a-Si layer can explain these results. First, the Source and Drain contacts are modified, as nc-Si is then no more in direct contact with the n+ layer. The main consequence is that under high field in the drain region, the contact does not behave as a poly-silicon-like contact, which, as explained previously, gives rise to band-to band tunneling and high leakage current. This explains the low leakage obtained on the bi-layer devices. In another hand, the presence of the a-Si layer on top of the channel acts as a passivation layer and prevents contamination of the nc-Si layer back side; which substantially improves the subthreshold region.

In the mean time, the ON-current is slightly lower on the device with the bi-layer, which can be explained by the increasing of the series resistance due to the presence of the additional a-Si at both Source and Drain ends. Overall, the use of the bi-layer structures appears to be very interesting for improving nc-Si devices.

Device stability: The shift of threshold voltage as a function of time during electrical stressing of the TFTs makes amorphous silicon TFTs unsuitable for use in AMOLED display without any additional compensation circuitry which penalizes strongly the open aperture ratio of the display. Stability of the nc-Si devices was then measured; by applying continuous voltages ($V_g$ = 12 V; $V_{ds}$ = 0.1 V) and measuring the drift of $V_{th}$ as a function of stress time, at different temperatures. TFT dimensions where still fixed at W = 400 and L = 20 µm. Figure 7 shows the evolution of threshold voltage shift for nc-Si TFTs (monolayer), in comparison with a-Si TFT devices. The experiment was made at 60° and 90°C. The results are summarized in Table 1.

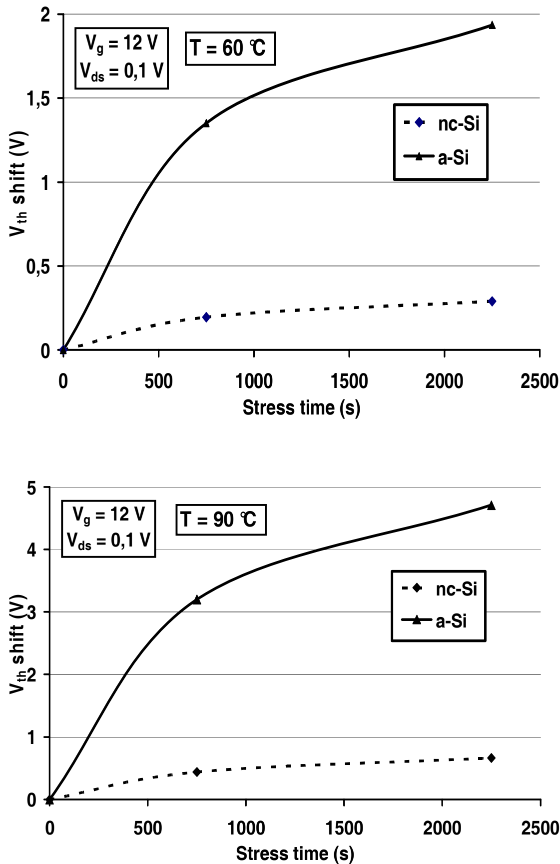


**Figure 7. Threshold voltage shift of nc-Si TFT under electrical stress at 60° (top) and 90°C (bottom). Stress conditions are: $V_g$ = 12 V and $V_{ds}$ = 0.1 V**

| | a-Si TFT | nc-Si TFT | $V_{th}$ shift improvement factor |
|---|---|---|---|
| $V_{th}$ shift at 60°C | 1,95 | 0,29 | 6,7 |
| $V_{th}$ shift at 90°C | 4,7 | 0,67 | 7 |

**Table I: Summary of $V_{th}$ shift measurements: $V_{th}$ shift after 2250 s of stress.**

From these results, it is clear that nc-Si devices are much more stable than their a-Si counterpart. For both temperatures, the voltage shift of nc-Si TFTs is around 7 times less than the voltage shift of a-Si TFTs. This result demonstrates the strong advantage of nc-Si over a-Si for the fabrication of AM-OLED backplanes.

## 4. Conclusion:

We obtained nc-Si TFTs which exhibit good characteristics such as high on-current and high $V_{th}$ stability. It has been evidenced that the use of a single layer of nc-Si can lead to degradation of the subthreshold area and of the leakage current, in particular under high negative Vg. In another hand, it was shown that by the addition of an a-Si layer between the nc-Si and n+ a-Si layers, the device performance is improved in the subthreshold area and the leakage current is drastically reduced. Stability of the nc-Si TFTs was evaluated by stress measurements carried out for different temperatures. When compared to similar a-Si TFTs, it has been shown that nc-Si provides a drastic improvement of the voltage threshold shift by a factor of about 7. The nano-crystalline silicon was deposited in a conventional Unaxis PECVD machine, and the devices were made using a standard bottom-gate, back-channel-etched process. Described TFT processing will provide a way to manufacturing of high performance AMOLED displays at a low cost.

## 5. Acknowledgements

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