2.22-inch qVGA a-Si TFT-LCD Using a 2.5 um Fine-Patterning Technology by Wet Etch Process

J. B. Lee, S. Park, S. K. Heo, C. K. You, H. K. Min, and C.W. Kim
MD Process Development Team, LCD Business
Samsung Electronics, KOREA
Phone: 82-31-209-8248, E-mail: juan.lee@samsung.com

Abstract

2.22-inch qVGA (240×320) amorphous silicon thin film transistor liquid active matrix crystal display (a-Si TFT-AMLCD) panel has been successfully demonstrated employing a 2.5 um fine-patterning technology by a wet etch process. Higher resolution 2.22-inch qVGA LCD panel with an aperture ratio of 58% can be fabricated because the 2.5 um fine pattern formation technique is combined with high thermal photo-resist (PR) development. In addition, a novel concept of unique a-Si TFT process architecture, which is advantageous in terms of reliability, was proposed in the fabrication of 2.22-inch qVGA LCD panel. Overall results show that the 2.5 um fine-patterning is a considerably significant technology to obtain higher aperture ratio for higher resolution a-Si TFT-LCD panel realization.

1. Introduction

Recently, higher resolution mobile TFT-LCD panels with higher aperture ratio have attracted a great deal of attention as the needs of customers for high-end LCD product increases. As a result, several attempts to realize a higher resolution mobile display have been made actively [1].

Above all, the use of fine patterning technology is inevitable to obtain a higher resolution mobile TFT-LCD panel [2]. Therefore, we have tried to apply a 2.5 um fine pattern formation technology using a wet etch process to 2.22-inch qVGA LCD panel production. Also, we have adopted high thermal PR with good thermal property and wet etchant with low side etch loss to fabricate a 2.5 um fine pattern-designed 2.22-inch a-Si TFT-LCD panel.

A novel concept of TFT process architecture where the direct contact between gate metal and data metal is possible, was proposed. Compared to the conventional process architecture, the proposed a-Si TFT process architecture is expected to have better reliability in high temperature and high humidity conditions because there is no ITO exposed-region in the top circuit area.

2. Results

In this work, a new concept of a-Si TFT process architecture was proposed. Using the total 6 mask TFT process architecture, we could successfully develop 2.22-inch qVGA a-Si TFT-LCD panel without additional mask step, compared to the conventional a-Si TFT process architecture.

In the case of conventional TFT process architecture, the contact between gate metal layer and data metal layer is formed indirectly through the bridge structure using an ITO layer. Therefore, this process architecture appears to be disadvantageous in terms of reliability because the ITO layer, acts as a bridge between gate metal and data metal, is exposed to the external environment.

On the other hand, the proposed a-Si TFT process architecture adopts the direct contact between gate metal and data metal layer through the CNT mask process. Considering these concerns, the proposed TFT structure using a direct contact between gate metal and data metal layer is more advantageous than conventional ITO bridge contact structure in terms of reliability.

In order to realize the 2.5 um fine patterning technology, firstly, we have partly remodeled the photolithographic equipment. By tuning the equipment, we can obtain a wider photolithographic margin for 2.5 um fine pattern formations.

In addition, a high thermal PR, which is known to have good thermal stability at high temperature, was used to fabricate 2.22-inch qVGA LCD panel. Figure 1 shows the cross-sectional SEM image of 2.5 um fine photo-resist (PR) patterns formed on the gate metal layer. As seen in Fig. 1, the 2.5 um space pattern (the gap between PR patterns) is definitely formed using the high thermal PR and the taper angle of the PR formed on gate metal layer is excellent. From SEM analysis, we observed that the taper angle of the high thermal PR was around 70°. It is confirmed that the adoption of the high thermal PR is very effective for 2.5 um fine pattern formations.

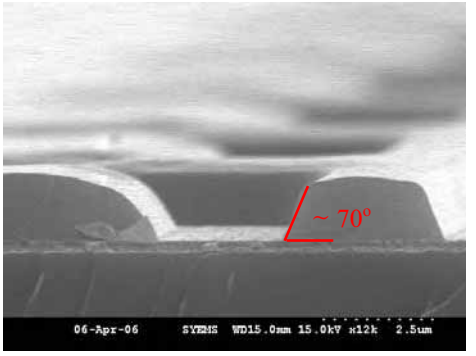

Figure 1. SEM image of the 2.5 um fine PR pattern using a high thermal PR

The thermal properties of PR used in the fabrication of 2.22-inch LCD panel were evaluated using a bake up to 140°C. Figure 2 shows the PR pattern before and after baking. Thermal re-flow of PR does not almost occur after baking up to 140°C. As can be seen in Fig. 2, there are no big differences (~ 5°) in the PR taper angle before and after baking at 140°C for 1hr. That is, the used PR exhibited good thermal stability, maintaining the original high contrast properties.

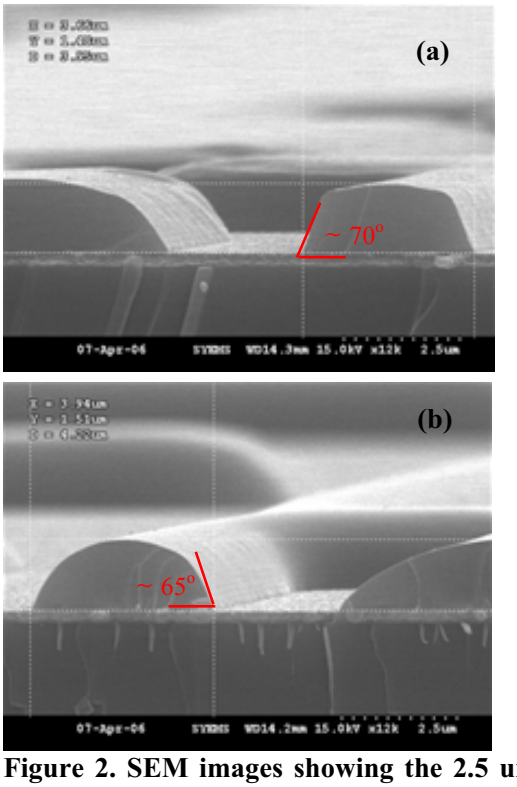

Figure 2. SEM images showing the 2.5 um fine PR pattern before (a) and after baking at 140°C for 1hr

We have checked the possibility that the side etch loss in the gate metal and data metal can be reduced by a wet etch process using a high thermal PR, compared to using a conventional PR. The side etch loss is defined as the difference between (A) and (B) in Fig. 3. When the high thermal PR was used, the side etch loss in the metal layer is approximately ~ 0.5 um, which corresponds to the half of that in the case of using a conventional PR. The improvement in the side etch loss is attributed to the basic properties of the high thermal properties. This phenomenon is deduced by that fact that the lifting of PR does not almost occur because the stress of high thermal PR is lower than that of conventional PR.

These results showed that the side etch loss of metal layer can be improved by a wet etch process using a high thermal PR, excellent in taper angle and thermal stability. Furthermore, the side etch loss by a wet etch process is expected to be more reduced by developing a wet etchant useful in the low side etch loss, in together with the high thermal PR.

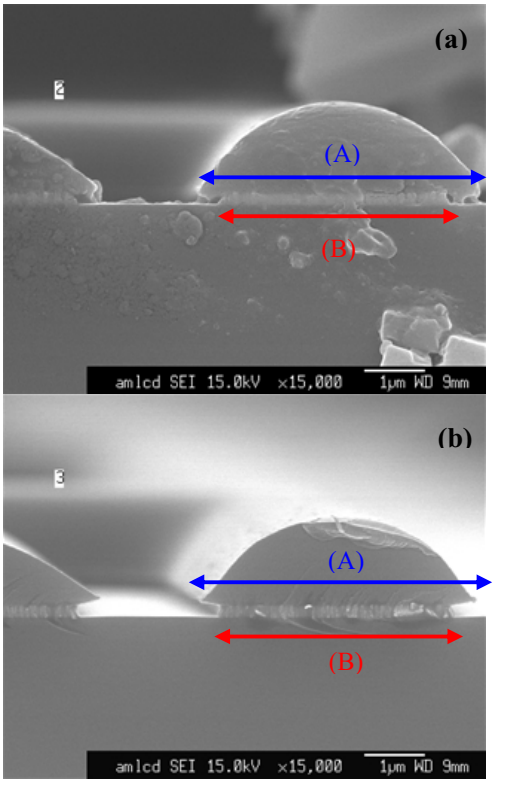

Figure 3. SEM images showing the side etch loss ((A)–(B)) of metal layer in the center (a) and edge area (b) in the glass after wet etching using a high thermal PR

We measured I-V characteristics of pixel TFTs in 2.22-inch qVGA LCD panels. Figure 4 shows the transfer characteristics of various pixel TFTs located in the glass substrate. As shown in Fig. 4, the stable TFT performances which meet the specifications of TFT characteristics can be obtained. Also, it is observed that there are no big variations of TFT performances such as Ion, Ioff and threshold voltage (Vth) in the glass substrates.

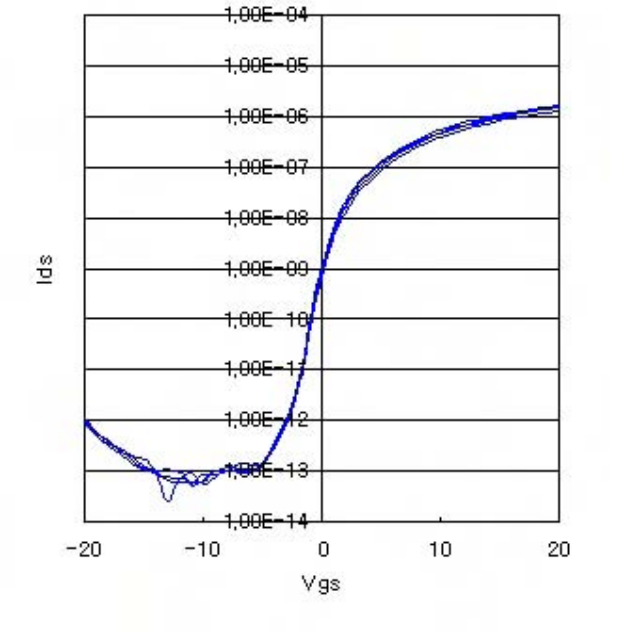

Figure 4. Transfer characteristics of pixel TFTs in the 2.22-inch qVGA LCD panel

Also, the 2.22-inch qVGA LCD panel where the direct contact between gate metal and data metal layer is formed, has been qualified in high temperature and high humidity driving conditions. It is confirmed that the new process architecture proposed in this report, is strongly effective to realize a-Si TFT-LCD panels with stable and durable reliability.

The demonstrated 2.22-inch qVGA a-Si TFT-LCD transmissive panel specifications are summarized in Table 1. As show in Table 1, we have obtained an aperture ratio of 58% by applying a minimum 2.5 um design rule to 2.22-inch qVGA LCD panel. As the minimum design rule for TFT-LCD panel changes form 4.0 um to 2.5 um, the aperture ratio of the TFT-LCD panel increased about a few %.

Table 1. 2.22-inch qVGA Panel Specification

Panel Size	2.22-inch
Pixel Density	180 ppi
Display Mode	Transmisive
Aperture Ratio	58 %
Display Area (mm)	33.84 × 45.12
Outline (mm)	37.64 × 54.16

Figure 5 is a display image of 2.22-inch qVGA a-Si TFT-LCD transmissive panel. High quality display image has been successfully implemented using a 2.5 um fine pattern technology.

Figure 5. Display image of 2.22-inch qVGA a-Si TFT-LCD.

Therefore, we conclude that the 2.5 um fine patterning technology adopting a high thermal PR gives rise to a strong rise in an aperture ratio of high resolution a-Si TFT-LCD. Additionally, it is confirmed that the proposed a-Si TFT process architecture, where the direct contact between gate metal and data metal is formed, is very effective TFT structure in reliability.

3. Conclusion

We have successfully produced 2.22-inch qVGA (240×320) a-Si TFT LCD panel using 2.5 um fine patterning technique. In the fabrication of 2.22-inch qVGA LCD panel, the side etch loss in the gate metal layer and the data metal layer is

reduced by a wet etch process employing a high thermal PR with good taper angle and thermal stability. In addition, the TFT process architecture proposed in this work, has demonstrated that it is advantageous in terms of reliability. Considering overall results, it is thought that the 2.5 um fine-patterning is a considerably important technology to realize higher aperture ratio for higher resolution a-Si TFT-LCD panel fabrication.

4. References

[1] R. Watanabe, O. Tomita, “Active-Matrix LCDs for Mobile Telephones in Japan”, *Information Display*, July 2003

[2] R. G. Stewart, “Circuit Design for a-Si AMLCDs with Integrated Drivers”, *SID Digest*, 1995