On the Cell Structure and Driving Method for High Efficiency Plasma Display Panel

Ho-Jun Lee*,Jung-Woo Ok, Don-Kyu Lee, Ji-Hoon Lee, Hae June Lee , Dong-Hyun Kim and Chung-Hoo Park

Dept. of Electrical Engineering, Pusan National University, Busan, Korea

Phone: +82-51-510-2301, E-mail: hedo@pusan.ac.kr

Abstract

Potentials and advantages of recently proposed raised bus electrode plasma display panel is discussed in terms of luminous efficiency, addressing speed. Detailed experimental and simulation results, which shows mechanisms of high efficiency driving mechanism, will also be given. Apart from the cell structure, we introduce new high efficiency driving method that can be applicable to conventional ac Plasma Display Panel.

1. Introduction

Plasma display is becoming one of the major large sizes, flat panel display in commercial television market. Recently the performances of PDP (plasma display panel) such as picture quality, reliability and efficiency have been improved greatly. However, there still are strong needs for further improvement of these performances in conjunction with true high definition format of 1920 by 1080 lines. Since the efficiency is expected to decrease with reducing pixel size, it is very important to develop the technology that can enable highly efficient driving of PDP. For high efficiency PDP, efforts have been done on the optimization of cell structures, gas blending and driving waveforms.

The use of long electrode gap and higher xenon partial pressure based on the conventional three electrode surface discharge structure is popular trends.[1-3] On the other hand, there have been interesting works on cell structure engineering based on the utilization of non- surface or modified surface discharge mode such as ridge structure and embedded bus electrode in the barrier rib have been reported.[4-6]

In driving ac PDP, temporal behavior of wall voltage set up and corresponding discharge current is one of the key factors in efficiency characteristics. The effective capacitance determined by dielectric layer is therefore very important parameter which affects the transient behavior of discharge and luminous efficiency. However, the studies concerning this subject are relatively limited, especially for experimental studies. By using the external capacitor, the effective capacitance between plasma and electrode can be reduced or controlled. Therefore, this can provide an experimental simulation of the effects of dielectric layer properties such as thickness or permittivity on the PDP performances.

With this background, we will discuss about the methods for high efficiency PDP in both the cell structure and driving point of view.

2. The cell design utilizing facing discharge modes

Fig. 1 shows an example of cell design that can utilizes a facing discharge modes. Layers of printed metal electrodes are sandwiched between dielectric layers. The number of layer and thickness of each layer is one of the design parameters that can control discharge current. The gap length between electrode edge from dielectric edge, which is also important for discharge current control should be optimize. The front panel was fabricated by successive printing, drying, etching, firing processes. During the firing process, etched dielectric layer flows and formed curved edge profile.

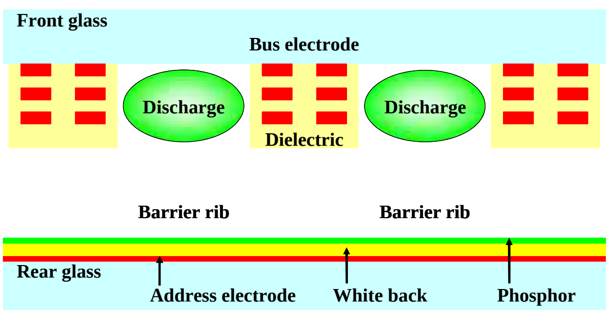

Fig.1 Design schematics of raised bus facing discharge cell (RBEPDP)

For the designed gap length of 370 μm, the actual gap length of each electrodes are measures as 320 μm , 340 μm and 390 μm from top to bottom of upper plate. The flow profile depends on the firing temperature and it is difficult to control precisely in multi layer electrode structure. Therefore, for the mass production point of view, it is desirable that the number of layer is minimized. The bottom electrode layer can be eliminated without losing our cell design concept. Second and third layer also can be merged with proper electrode thickness. In this case, the height between front glass and electrode become important parameter.

We fabricated RBEPDP having different discharge gap length as 300, 330, 350 and 370 μm. To compare the performance of proposed structure with conventional PDP cell, RBEPDP conventional PDP cell was fabricated in the same panel.

For the barrier rib structure, closed type for reference cells and stripe type for RBEPDP were used. In RBEPDP, the rib area between the electrode is etched away to maintain gap length between front and rear glass at the height of barrier rib (190 μm). Discharge Gap length of the reference cell is 60 μm and the thickness of dielectric thickness is 30 μm. Xe (8 %) – Ne binary gas mixture is used as working gas and the base pressure is 400 Torr. The cell size is 300 by 676 μm, which correspond to the dimension of one sub pixel in 42” PDP with XGA resolution. The test panels are 4” Monochrome green and all the sustain drivings are done under the continuous square voltage pulses of 10KHz, 25% duty ratio.

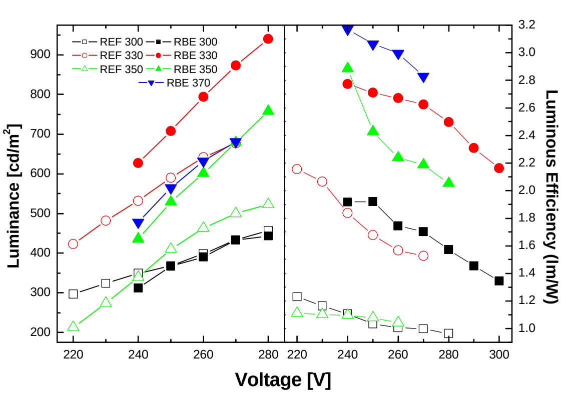

Fig.2 Luminance and Efficacy Characteristics of RBEPDP

Luminance and luminous efficiency characteristics of RBEPDP are shown in Fig. 2. RBEPDP samples have higher or similar luminance value compared with its reference cells in spite of their low charge current. Average increment of luminance is estimated as about 15%. Since RBEPDP have high luminance and low current characteristics, efficiency increases drastically. Resulting efficiency improvement is ranged from about 60 % to over 100 %. Efficiency improvement without loss of luminance is important for the application point of view.

3. High efficacy driving with external current ballast capacitor

Fig.3 shows schematic drawing of experimental setup. Simple sustain circuit consist of four IR840 switching devices. PDP is represented as four equivalent capacitors and one current source. External ballast capacitor is inserted between sustain electrode and ground. The capacitance should be chosen so as to generate proper blocking voltage during discharge, which depends on the number of ON cells. We have used 4” test panel. The dimensions of pixel correspond to XGA resolution panel having 42” diagonal size. Closed type barrier rib structure has been used. Total number of display pixel is ranged from 700 to 1400.

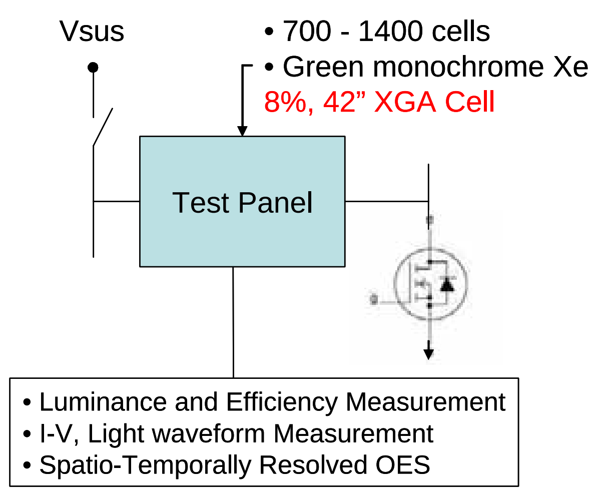

Fig. 3 Experimental setup for driving with external ballast capacitor

In this load range, the output capacitance of the IR840 itself, which is ranged from 250 ~ 100 pF for drain to source voltage of 10 ~ 50 V, can provide the proper ballast function. By turning off the switch 2 and 4 when the sustain voltage is applied through switch 1 and 3, scan and common electrode is successively floated and capacitively coupled with output capacitance of IR840 devices.

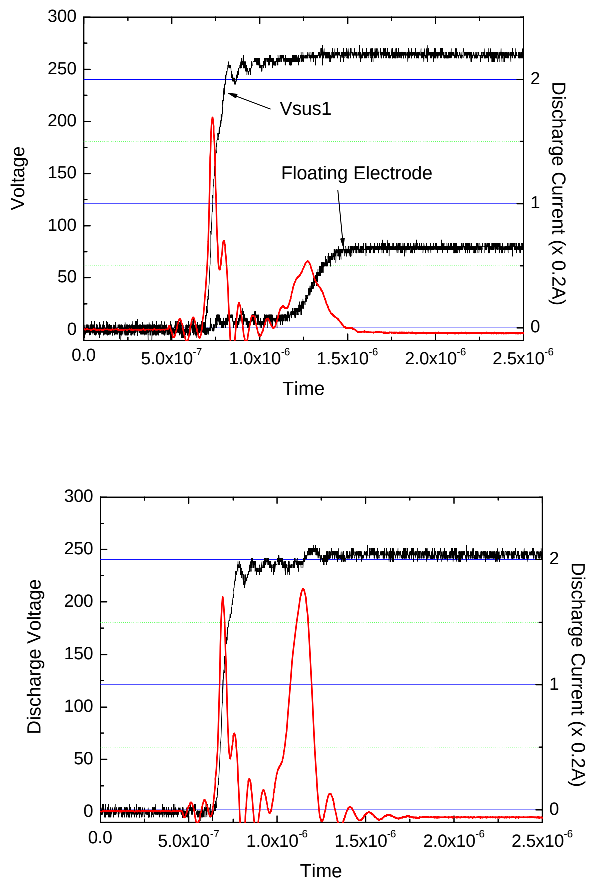

Fig. 4 Current and voltage waveform for floating and normal mode driving

Fig 4 shows current and voltage waveforms for floating mode which correspond to driving with external capacitor. The number of discharge cell was 1400. For the floating mode, small voltage increment at the floating electrode is found due to displacement current flow. When the discharge is initiated and discharge current begins to flow, voltage at the floating electrode increases due to charging of ballast capacitor. Consequently gap voltage is decreased much faster than that of normal driving mode. This limits the fast grow of discharge current. The peak current level also dramatically reduced compared with normal mode. The same effect may be expected on the gap voltage increment when the effective capacitance of dielectric layer is decreased. Peak discharge current of floating mode can be reduced down to 30 % of current peak of normal modes. On the other hand, the discharge duration is increased by 50 % compared with that of normal mode.

Decreases in the total discharge current may give similar effect on the current waveform as increases in the capacitance of the ballast capacitor. When the panel load is decreased by 50 %, the current limit function of ballast capacitor becomes ineffective due to lower voltage increment of floated electrode. It should be noted that since the output capacitance of switching device is higher at lower source to drain voltage, the relative current reduction capability at the lower load is underestimated compared with that in fixed ballast capacitance case.

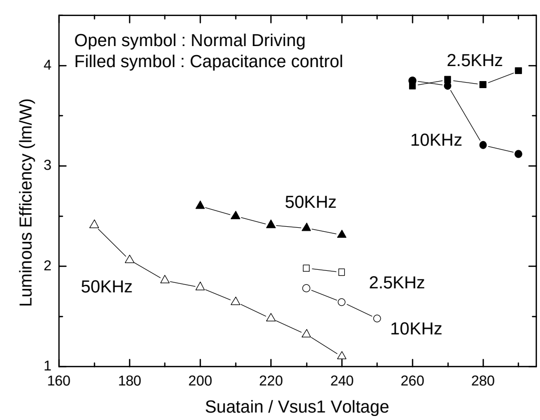

Fig.5 Luminous Efficacy characteristics

Fig. 5 shows measured luminous efficacy as a function of driving voltage and frequency when the total number of discharge cells is 1400. In both cases, power consumption increases with sustain voltage. No conspicuous difference is found with driving frequency. In floating mode, power consumption is 2-3 times lower that that of normal mode greatly reduced for all cases. On the other hand, luminance is decreased by about 30 %. The increasing rate of power consumption with sustain voltage is lower in floating mode. The improvement ratios in luminous efficacy are ranged from about 50 % to 200 %.

When the panel load is half of the previous case, the degree of luminance enhancement is very limited. This tendency is easily expected from the results in Fig.2, which is due to the fact that the voltage rising of capacitively coupled electrode is proportional to the total discharge current of the panel

4. Conclusions

We proposed and fabricated PDP having vertically raised multi layer bus electrode. RBEPDP shows higher luminance and luminous efficiency simultaneously compared with those of conventional PDP structure. Experimental results show that these improvements come from higher excitation efficiency, larger plasma volume and lower surface loss of charged particles.

The effects of external capacitance on the discharge characteristics of ac PDP have been investigated. The fast rising of gap voltage due to charging of external capacitor makes the peak discharge current lower and the discharge duration longer. These changes of transient behavior result in high luminous efficacy.

Since the role of external capacitor is almost the same as that of the dielectric layer of the ac plasma display panel except that it responds to the whole panel current, the results present in this study such as current waveform and efficiency characteristics can be applied to infer the effects of dielectric layer of the ac PDP.

.

5. Acknowledgements

This work was supported by 21C Frontier Next Generation Information Display Development Program.
This work was also supported by LG electronics

References

[1] L.F. Weber, Proceedings of 23rd International Display Research Conference, 16-18 September 2003 pp, 119-124

[2] D. Hayashi, G.Heusler, G. Hagelaar and G. Krosen, J. Appl. Phys, **95**, 1656 (2004)

[3] G. Oversluizen, M. Klein, S.de Zwart, S. van Heusden and T. Dekker, J. Appl. Phys, **91**, 2403 (2002)

[4] S.-H Son, Y.-S Park, S.-C Bae and S.-Y Choi Appl. Phys. Lett. **80**, 1719 (2002)

[5] M.-H Nam, S.-Y Choi, S.-H Son and Y.-M Kim, J. Appl Phys. **97**, 73304 (2005)

[6] H. Asai, S.Ajisaka, S. Mori, A.Oku, K.Ikesue, S. Moei, K.Tanaka, N.Kikuchi, M. Hiroshima, S. Sakamoto, Proceedings of International Display Workshop, 2003, pp. 897-900

[7]J.W. Ok, H.J. Lee, W.S. Choi, Y.M. Jang, H.J. Lee and C.H. Park "A Study on the Characteristics of AC-PDP with Stacked Facing Electrode" IDW'05