New electrical test method for LCD cell manufacturing process

Yasuhiro Miyake*, Kiyoshi Chikamatsu
Masaharu Goto, Junichi Mizoguchi
Agilent Technologies International Japan, Ltd., Hachioji-shi, Tokyo, Japan
Phone:+81-42-660-3122 , E-mail: yasuhiro_miyake@agilent.com

Abstract

We propose a new electrical test method bringing repeatable and unambiguous test results eliminating drawbacks of the lighting test for LCD Cell manufacturing process. In this paper, we will show its basic concept, examples of actual test results and effectiveness of the method.

1. Objectives and Background

In the TFT array manufacturing process, highly repeatable defect detection and quick process feedback are achieved by fully automated test using array testers[1].

On the contrary, in the LCD cell manufacturing process, in few cases automated lighting test with CCD camera[2] is adopted, but in most cases lighting test with human eyes are used.

Lighting test with human eyes has issues on test repeatability and the ambiguity. Especially in MURA detection, it is difficult to obtain reliable and consistent test result, because the MURAs have many different shapes and sizes and the test results depend on human perceptions[2]. The automated lighting test with CCD camera is effective for large-area MURAs but have some difficulties in detecting a line MURAs and pixel defects because of a pixel-resolution difference between the CCD camera and the panel under test. Moreover, the lighting test fundamentally cannot detect specific sort of defects such as a mobile foreign materials inside liquid crystal (LC) layer, which may be hidden behind a non-display area during the test and then move to a display area after being delivered to the market.

Nowadays panel users request quality assurance, hence objective test criteria are desired in the LCD manufacturing process. However, as designed pixel size becomes smaller, detection of small defects becomes more and more critical. Sensitivity of human eyes may limit the test capability for high resolution panels.

In this paper, we propose a new electrical test method bringing repeatable and unambiguous test results which eliminates the drawbacks of the lighting test described above. We will describe the test scheme and wide test coverage of the proposed method, and show the example of the actual measurement result.

2. New test method theory

In the LCD cell process, there are many types of defect modes such as foreign material inside liquid crystal (LC), cell-gap defect, ITO patterning error, color filter (CF) crack, alignment layer defect and injection port MURA. Those defect modes affect LC transmission, and simultaneously affect either the dielectric constant between ITOs (pixel ITO and common electrode ITO) or the distance between ITOs or the size of ITO or the transient property of LC. All of those effects cause the variation of the capacitance value between ITOs.

The new cell electrical test method proposed in this paper is to detect defect pixels with the variation of measured capacitance values and distinguish those defective pixels into a relevant defect mode.

As mentioned above, all types of the defect modes affect the capacitance value between ITOs, and those defect modes can be categorized into 2 types by the sort of the effect on LC property. Defect modes such as foreign material inside LC, cell-gap defect, ITO patterning error and CF crack affects only LC “static” properties like dielectric constant, distance and size. On the contrary, the defect modes such as alignment layer defect and injection port MURA, affecting LC “transient” property.

The proposed method contains 2 types of the test procedure. The first procedure (Procedure-I), specializing in the “static” defect modes, utilizes the state characteristic of LC[3], and the second one (Procedure-II), specializing in the “transient” defect modes, utilizes the transient characteristic of LC[4].

The basic scheme and the test coverage of the each procedures are described below.

2-1. Procedure-I : using the state characteristic of LC

Procedure-I is used to detect defect modes such as the foreign material inside LC, the cell-gap defect, and the ITO patterning error and the CF crack.

Test step of Procedure-I is as follows:

1) Apply a certain electrical field to the LC and wait until transient state of LC settles.

2) Measure the capacitance value of the LC.

Test principle of each defect mode detected with Procedure-I is as follows:

1) Foreign material inside the liquid crystal layer

Sealant and glass particle can sneak into LC layer as foreign materials. Those materials have different dielectric constant from LC, then if there is a foreign material inside the LC layer, the capacitance value between ITOs is affected. Normally, the dielectric constant of the sealant and the glass particles are smaller than that of the LC under high electrical field. In order to detect the defect caused by foreign materials precisely, the capacitance value has to be measured after liquid crystal dielectric constant settles under high electric field conditions.

The effect mentioned above is caused by a foreign material particle whose diameter is smaller than the cell-gap. When there is a foreign material whose diameter is larger than the cell-gap, that foreign material exerts outward pressure against the glass walls causing the cell-gap to bulge around that foreign material. Hence the capacitance value of that area is then smaller than the capacitance value with a normal cell-gap distance.

2) Cell-gap defect

When there is a cell-gap difference between the center area and the edge area of the panel, we can also observe it as a capacitance value difference between those areas. For example, assuming cell-gap nominal value of 4um with an error tolerance of plus or minus 0.1um, if there is 2.5% difference in measured capacitance value between the center and edge area, we can know that panel has cell-gap defect.

3) ITO patterning error and Color Filter crack

When there is a crack in the ITO or the CF, the capacitance value between ITOs is smaller than the capacitance value for good pixels (Here, we are defining a “good pixel” as a defect-free pixel.). ITO cracks decrease the ITO area, causing smaller capacitance value, and Color Filter cracks increase the distance between ITOs, causing a smaller capacitance value. On the contrary, if a certain pixel ITO area is larger than the ITO area for good pixels caused by ITO under etching, the capacitance value for that pixel is larger than the other good pixel values.

2-2. Procedure-II : Utilizing the transient characteristic of LC

Procedure-II is used to detect defect modes such as an alignment layer defect and LC Injection port MURA.

LC molecules take on the order of millisecond to change direction after a change in electrical field. However the transient time varies depending on alignment layer (PI-film) and LC transient properties. If there is a PI film defect, the transient period of that pixel is longer than that of good pixels. Additionally, if there are excessive ions inside the LC layer, the transient period of that area is longer than that of good pixel areas.

The LC dielectric constant depends on the direction of the LC molecule, and the capacitance value between ITOs depends on the liquid crystal dielectric constant. Hence the transient property deviation of LC can be seen by measuring the capacitance value between ITOs while LC molecules change their direction.

Test step of Procedure-II is as follows:

1) Change the direction or strength of the electrical field on LC,

2) Measure the capacitance value of the LC while LC dielectric constant is changing.

Test principle of each defect mode detected with Procedure-II is as follows:

1) Alignment layer defect

The alignment layer defect can occur if there is a defect in PI coating, pre-curing, baking or rubbing processes.

For example, if there is a PI film hole (crack) on the alignment layer, the liquid crystal transient period of that pixel is longer than the good pixel transient time. The high electrical field is applied between ITOs and kept for a certain period before measuring capacitance. At the time of the measurement, the dielectric constant of the defective pixel is different from that of the good pixel.

If there is a defect in the rubbing process, the shape of the defect area is observed as diagonal lines. With that knowledge, the rubbing defect can be identified from other defects.

2) Injection port MURA

Around the injection port, inside the liquid crystal layer there tends to be excessive ions from injection port sealing material. These excessive ions make the liquid crystal transient period longer.

Injection port MURA can then be identified by shape and location from other defects.

2-3. Required measurement sensitivity

Required measurement sensitivity to detect each defect mode is shown in Fig.1. Where 2.4'' QVGA panel is assumed. 3.5fF to 11fF measurement sensitivity is necessary to detect these defects. In order to perform this kind of highly sensitive measurement, an extremely high performance array tester is indispensable.

The validity of our new test method has been proved using the Agilent 88000 HS-100 array test system. Since HS-100 measurement sensitivity is better than 1fF (Fig.1), an accurate validation can be performed.

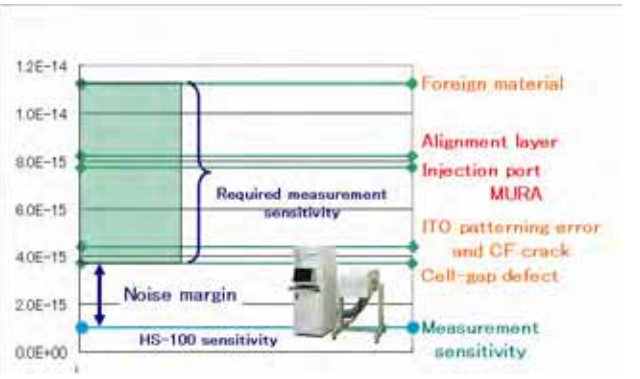

Fig.1 Measurement sensitivity and test coverage

(Vertical axis: sensitivity (standard deviation) [F])

3. Example of the actual data

To show the effectiveness of the proposed test method, the actual measurement result of Procedure-I are shown in Fig.2-1 and 2-2. These measurement data are obtained from Agilent 88000 HS-100.

Fig.2-1 shows a 2-dimensional map of the measured capacitance data arranged in the same form of actual panel. Here the brighter data means larger capacitance values and darker data means smaller capacitance value. Fig.2-2 shows a capacitance map of an emulated cell-gap defect. We used the same panel as Fig.2-1, and pressed on the left center of the panel surface with an elastic material so that the glass surface deforms partly like a crater. The distance between ITOs of the pressed area in the condition of Fig.2-2 is shorter than the distance in the condition of Fig.2-1, then the capacitance value of that pressed area in Fig.2-2 becomes larger than the capacitance value in Fig.2-1.

Fig.2-3 is achieved by subtracting capacitance values in Fig.2-1 from those of Fig.2-2. The pressed area can be recognized as a brighter region, where the maximum deviation is about 2.5% of the capacitance value and corresponds to the same order of cell-gap deformation. This result clearly shows that the proposed test method can detect cell-gap defects by measuring the capacitance value between ITOs.

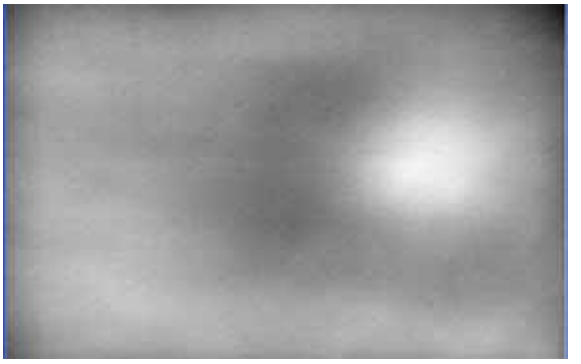

Fig.2-1 Panel map of Capacitance Measurement value (defect-free panel)

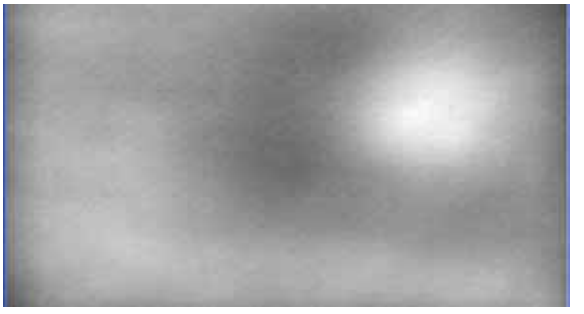

Fig.2-2 Panel map of Capacitance Measurement value (panel pressed partially.)

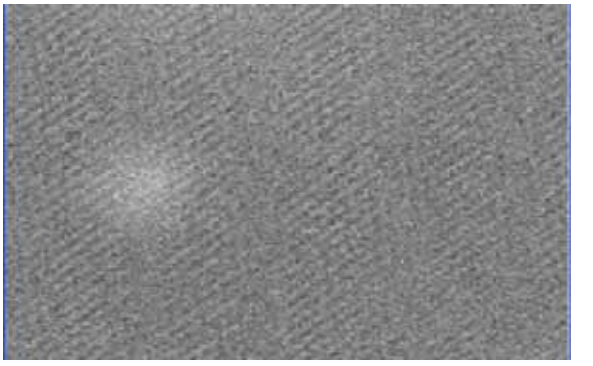

Fig.2-3 Panel map of Capacitance Measurement value(The difference between Fig.2-1 and Fig.2-2. That point can be seen as a bright area on the left center.)

4. Conclusion

In this paper, we proposed a new test method for the cell manufacturing process that can be applied to any type of LCD panel. Furthermore, we showed its effectiveness in detecting defects with the objective numerical terms, drastically improving the drawbacks of the lightning test with human eyes.

5. References

[1] R. Wisnieff et al, SID 90 Digest, p.190 (1990).

[2] Yumi Mori et al, IDMC 2003, P.295 (2003)

[3] Patent pending.

[4] Patent pending.