Novel high speed and sensitivity array test system for LTPS LCD and OLED

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Abstract

The high speed and sensitivity array test system has been developed and utilized for mass-production of advanced LTPS displays including SOG and OLED. It realizes fast enough TACT enabling 100% inspection with better than 1fF sensitivity. The result of actual measurement shows its superior TACT and sensitivity, and also shows MURA detection of OLED panel.

1. Objectives and Background

The evolution of the LTPS process technology has enabled displays with highly integrated circuit, called SOG[1][2], and LTPS based OLED, for which high volume mass-production is highly expected to start in 2007[3].

However, these high-end display devices suffer from the price competition against low-priced a-Si devices and continuous yield improvement in array process is essential. With those backgrounds, the requirements for today's array test in LTPS manufacturing are described as follows; 1)High throughput applicable to 100% inspection in high volume production 2)Sure detection of both clear and weak defects in pixel 3)Process feedback using array test results 4) test recipe for quick ramp up of new product testing 5) Test capability for a variety of integrated circuits, such as DAC, DC-DC converters etc. 6)High sensitivity measurement capability for future devices having smaller capacitance 7)Test solution for narrow pad-pitch and high pin-count COG panels 8)EL driving TFT test for OLED before or after EL deposition 9)Recommendation on better Design For Testability(DFT) circuitry for effective testing.

2. Developed test system

Agilent 88000 HS-100(Fig.1) has been resolving all of the above requirements under the cooperation with glass prober and probe unit suppliers, and are being utilized in the high volume manufacturing sites.

The HS-100 test system is configured with analog modules to measure pixel characteristics and digital modules to output or input digital signals for panel under test. In particular, the high sensitivity is realized by charge integration with low noise amplifier and fully guard shield for signal paths, as well as special cares to reduce noise from electro-magnetic coupling with external noise source, such as power lines. The tester hardware is uniquely designed combining low current measurement technology and digital test technology based on vector pattern sequencing. Each technology is well familiar among either semiconductor parametric or SOC testing for silicon devices.

3. Performance of test system

3-1. Measurement sensitivity and test time

To demonstrate the tester performance for some of the above requirements, OLED panels on the market were actually measured on the electrical characteristics using HS-100. Basic performance curve of sensitivity v.s. measurement time is obtained for pixel capacitance test in QCIF+ formatted, point-scan, and 2T/1C type OLED panel as in Fig.2, where measurement repeatability, expressed in standard deviation, is less than 1fF(femto farad, 10^{-15}F) at less than 1 sec/panel test time. The measurement resolution of 1fF means the tester can discriminate 5fC charge difference in storage capacitor charged at 5V and it is equivalent that it can discriminate 5fC/500fF=10mV difference in the storage node voltage, when storage capacitor is 500fF.

3-2. Pixel charge measurement

Fig.3 is the pixel capacitance map obtained by measuring storage capacitance(Cs) and gate-to-

source capacitance(Cgs) of EL driving TFT together in each sub-pixel. Pixel capacitance value averaged over the panel is 751fF. Although the variation allover the panel has the standard deviation (σ) of only 1.5%(=11fF/751fF), even small fluctuation can clearly be observed and is considered to reflect process non-uniformity.

Fig.4 shows design verification capability of HS-100 for pixel stray capacitance. One of the important tasks for TFT circuit designer is to predict small parasitic capacitance around the storage node, including gate-to-source capacitance of switching TFT. However, asymmetry in pixel design may raise the parasitic's asymmetry as well, and it may affect the device operation. Such asymmetries can be seen, for example, in RGB-delta tiling in Fig.4(a). Cs+Cgs distribution in the vertical direction for this tiling panel is measured as in Fig.4(b) which shows around 10fF difference in odd and even row capacitance values.

The quasi static C-V curve in Fig.5 is measured for Cs+Cgs for all the sub-pixels and the data suggest the threshold voltage is just over Vgs=2V [4]. This measurement is useful when non-uniformity in threshold voltage is of primary concern.

3-3. OLED panel MURA detection

OLED current is also measured applying current measurement function of HS-100 and the resulted map is compared with light-on image taken by digital still camera.(Fig.6) A weak point defect and many horizontal streak MURAs are found in the same positions. The good match is naturally associated with highly linear relationship between the EL current and luminance. The horizontal MURA can be related to TFT characteristic variation due to the laser anneal process variation.[5][6]

3-4. Pixel defect analysis

In order to ramp up mass-production and reduce manufacturing cost, the yield management of TFT array is significantly important. For the purpose of quick yield improvement, a reliable analysis tool and right methodologies are the keys in detecting true cause of defects.

Here, an example of defect analysis is simply introduced using the device with a defect at (X,Y)= (77G,172). (Fig.6)

Firstly, |Vgs| v.s. $\sqrt{\ }$Ids curve is obtained as in Fig.7, which compares a defective pixel at (77G,172) and normal pixels(panel average). From this chart, 75mV of threshold voltage difference may be suspected of the cause. But this difference in a static device parameter doesn't explain the reason why EL current decays in the dynamic driving waveform (Fig.8).

To investigate more deeply, the charge retention characteristic [7] is measured as in Fig.9. According to this chart, it is understood that as retention time is extended, the stored charge is more remarkably lost at the defective pixel and this clarifies there may be a shorting path between both ends of the storage capacitor.

4. Conclusion

The novel array test system is introduced and the quantitative test results show enough sensitivity as well as short test time. Future trend in LTPS will lead to more pixel density having smaller capacitors and more circuits inside the panel. HS-100 test performance will surely help yield ramp up and cost down in LTPS array process.

6. References

[1] T.Matsuo, et al., SID'04 Digest,p856(2004)

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[3] http://www.oled-info.com/newsArchive/January2006.html

[4] S.W.Tam, Ph.D thesis,Cambridge univ.(1994)

[5] J.W.Hamer, et al.,SID'05 Digest,p1902 (2005)

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Fig.1 Agilent 88000 HS-100 array test system

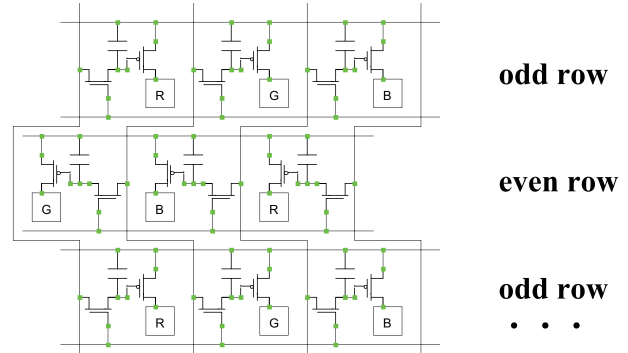

Fig. 4(a)

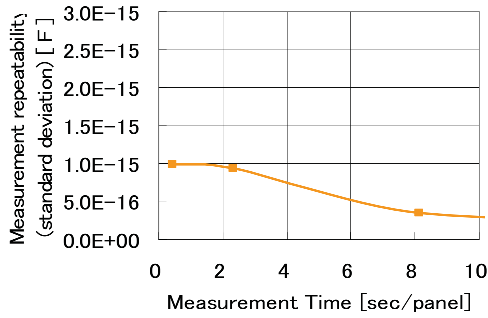

Fig.2 Sensitivity and measurement time

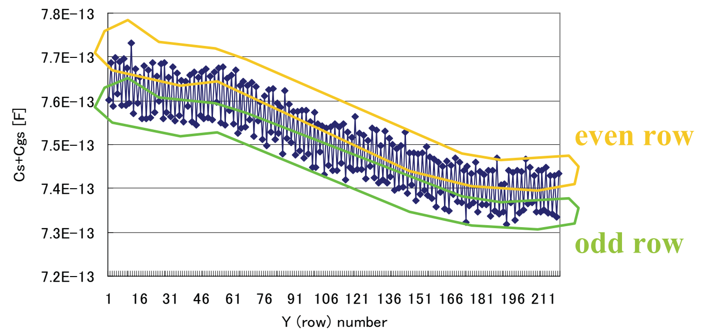

Fig. 4(b)

Fig.4 Explanation of capacitance difference in even/odd row in RGB-delta pixel tiling

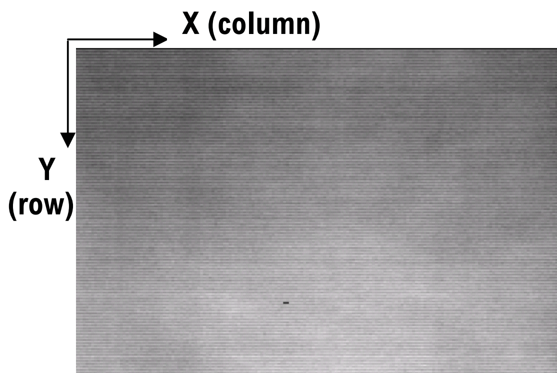

Fig.3 Pixel capacitance map

(average=751fF/2sub-pixels , σ=11fF)

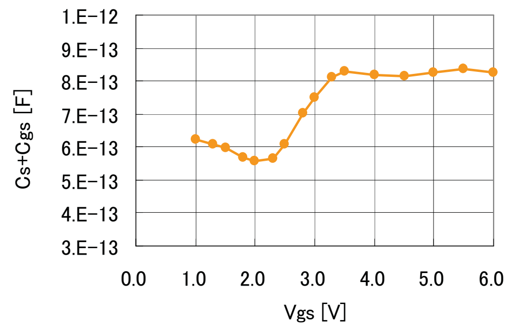

Fig.5 C-V curve for OLED pixel capacitance

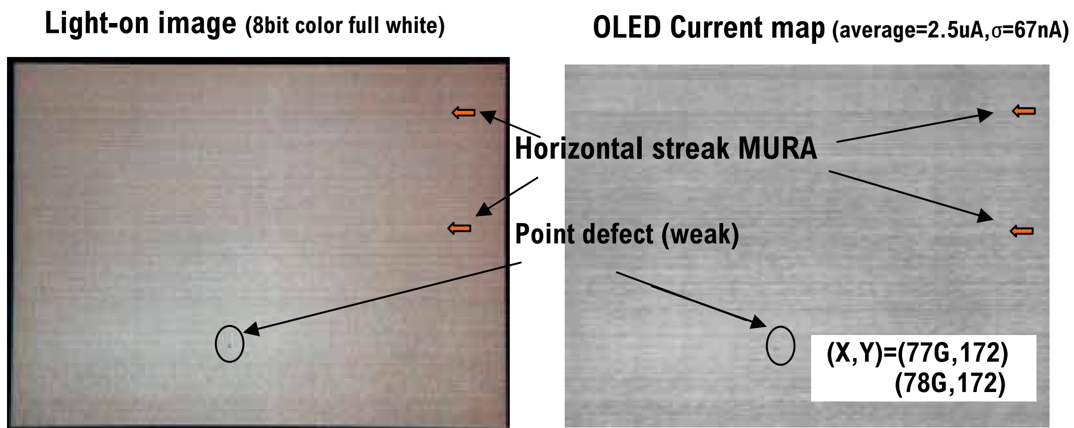

Fig.6 Light-on image v.s. OLED Current map

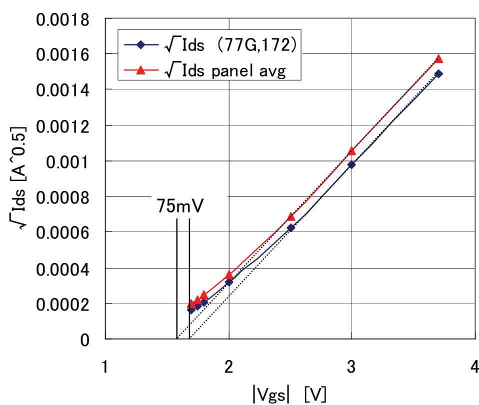

Fig.7 |Vgs| vs √Ids curve for darker pixel at (X,Y)=(77G,172) and panel average

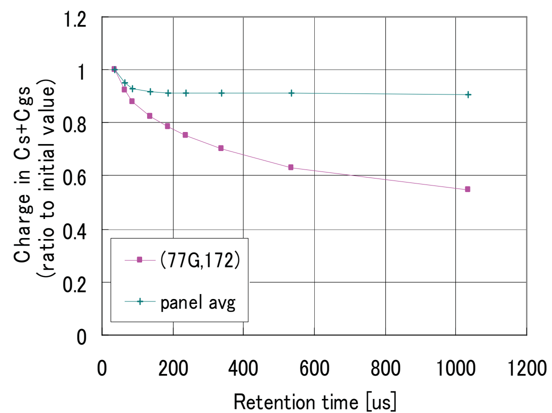

Fig.9 Charge retention characteristic for darker pixel at (X,Y)=(77G,172) and normal pixels(panel average)

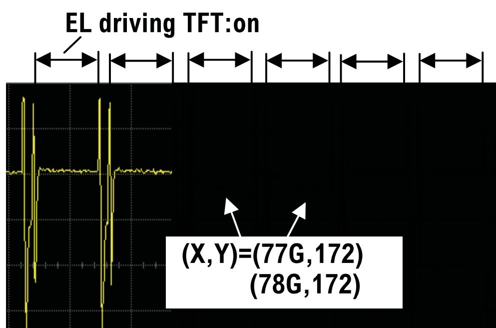

Fig.8 OLED drive current waveform around defective pixel (vertical:10uA/div,horizontal:200us/div)